Small-Signal Modeling of RF CMOS

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Abstract

This paper presents accurate small-signal modeling of RF CMOS, valid from DC to GHz ranges, using device simulation and analytical modeling. Distributed NQS effects in terms of circuit parameters are discussed and an estimation of the limit up to which quasi-static MOSFET models are reasonable is presented. The impact of the substrate network through g_{mb} multiplication on terminal ac characteristics is also discussed.

I. Modeling and Analysis

Calibration of the process simulator is done using SIMS to generate a two-dimensional device structure. IV characteristics are also calibrated using mobility parameters, Lombodi model, and suitable semiconductor workfunction. Once the process is calibrated, device structures with different channel length (L = 50 um, 10 um, 2.5 um, 1.2 um, 0.6 um, 0.3um, and 0.15 um) are generated using the process simulation. For each device, all sixteen y-parameters, y_{gd}, y_{gs}, y_{gb}, y_{dg}, y_{ds}, y_{db}, y_{sg}, y_{sd}, y_{sb}, y_{bg}, y_{bd}, y_{bs}, y_{gg}, y_{dd}, y_{ss}, and y_{bb}, are simulated for all bias regions ($0 < V_{DS}$ & $V_{GS} < 3$ V) from 10 Hz to 60 GHz.

The development of a small-signal model is based on the well known general four terminal y-parameter network as shown in Fig. 1a. The characteristic of each y-parameter in Fig. 1a is represented as a circuit form by analyzing the frequency response.

An often mentioned problem in RF CMOS modeling is non-quasi-static phenomena. It is reported that this NQS effect occurs most dominantly in C_{gg} and g_{gg} parameters as shown in Fig. 2 where gate capacitance, C_{gg}, degrades at high frequencies and the conductance increases proportionally to f^2, which is directly related to induced gate noise. However, NQS effects on bias dependency of individual modeling parameters (i.e., C_{gs}, C_{gd}, C_{sd} etc.) are not well known. Fig. 3 shows the bias dependency of C_{gs} and C_{gd} for L = 1.2 um device at frequencies of 6.5 GHz and 17 GHz. In the linear region, the amount of degradation of C_{gs} and C_{gd} between 6.5 GHz and 17 GHz is the same but in the saturation region, $V_{DS} = V_{GS} = 3$ V, the degradation of C_{gs} is significant while C_{gd} shows little degradation. This is due to the effective channel length, L_{eff}, of C_{gs} and C_{gd} which is bias dependent due to charge sharing as illustrated in Fig. 4. Thus the effective channel length is related as:

$$L_{eff-gs} \cong L \cdot \frac{C_{gs}}{C_{gs} + C_{gd}} \tag{1}$$

For short channel devices, the NQS frequency, f_{NQS}, where the capacitance starts to degrade can be formulated as:

$$f_{NQS-C_{gs}} = n\left[\frac{\mu(V_{GS}-V_T)}{2\pi L_{eff}^{\ 2}}\right] \quad (2)$$

Where n is a fitting parameter. Similarly f_{NQS} for C_{gd} can also be formulated.

The substrate network from drain and source terminals can be represented as parallel RC circuits, R_s and C_s, as shown in Fig. 5a. This substrate network accurately represents the frequency response of source to bulk and drain to bulk. Extracted substrate parameters for both drain and source sides for all biasing regions are shown in Fig. 6. It is very interesting to note that the extracted substrate parameters, R_{s_drain}, R_{s_source}, C_{s_source}, and C_{s_drain}, show the following conservative behavior.

$$R_{s-drain}C_{s-drain} = R_{s-source}C_{s-source} \quad (3)$$

This relationship is due to the material property of the lossy silicon substrate, dictated by

$$R_sC_s = \frac{\varepsilon_{si}\varepsilon_o}{\sigma_{si}} \quad (4)$$

Simulated terminal capacitances of a long channel device, in Fig 7a, follow the same characteristics of intrinsic capacitances derived from the charge-based model. However, C_{ss}, C_{sg}, C_{sd}, and C_{sb} for short channel device, in Fig. 7b, show significantly different characteristics (i.e., the capacitances are multiple values of maximum gate capacitance as high as 53 times). This is due to the existence of the substrate resistance and g_{mb} as:

$$C_{sdeff} = C_{sd} + \frac{R_{sub}g_{mb}}{1+\omega^2R_{sub}^2C_{bb}^2}C_{bd} \quad (5)$$

likewise, the effective source to drain conductance is:

$$g_{sdeff} = g_{sd} + \frac{\omega^2R_{sub}^2g_{mb}}{1+\omega^2R_{sub}^2C_{bb}^2}C_{bb}C_{bd} \quad (6)$$

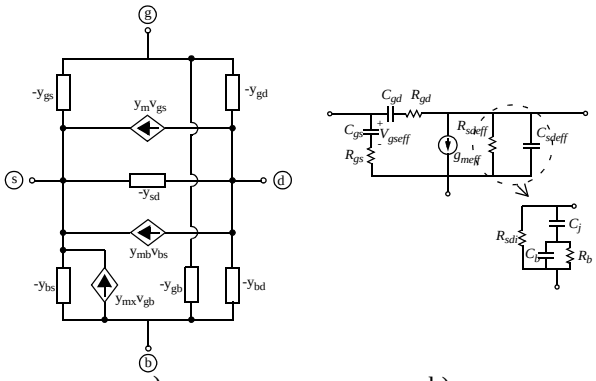
Where the R_{sub} represents substrate resistance as shown in Fig. 5b. C_{ds}, C_{dg}, C_{ds}, and C_{db} show similar behavior. Since both g_{mb} and R_{sub} are proportional to 1/L, the g_{mb} amplification (second term in Eq. 5~6) occurs increasingly for short channel devices. At high frequencies, the second term in Eq. 5~6 disappears and only intrinsic term remains. Fig. 8 shows that the intrinsic term C_{sd}, which is negative for long channel device at linear region, becomes positive as channel length decreases. It is reported [2] that this is caused by DIBL effects. This work shows that this dependency is mainly a geometrical effect as source and drain junction capacitance becomes dominent while intrinsic C_{sd} decreases as L decreases.

For the common-mode configuration, the simple compact model accounting for the NQS effect, g_{mb}, and the substrate effect is developed, in Fig. 1b, resulting in error of less than 2% in terms of s-parameters for all biasing regions from DC to GHz range.

References

[1] Y. Tsividis, *Operation and modeling of the mos transistor*, McGraw-Hill, second edition, 1999.

[2] M. Je, H. Shin, SISPAD, 2003. SISPAD 2003, pp.247-250, September 2003.



a) b)

Figure 1: a) general y-parameter network of four terminal MOSFET. b) Simplified small-signal model for common source configuration.

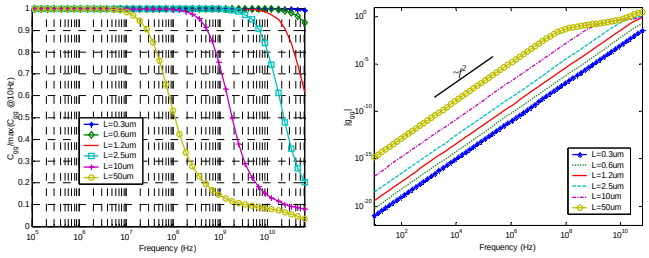
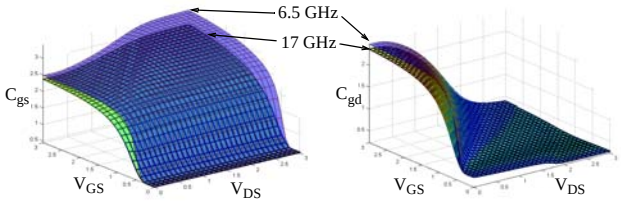
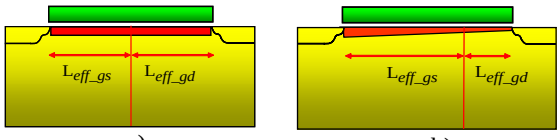


Figure 2: Simulated C_{gg} and G_{gg} vs. frequency for various channel length at V_{DS} = 0 and V_{GS} = 3 V. The C_{gg} is normalized by the maximum C_{gg} at 10 Hz for each device. Both C_{gg} and G_{gg} degrade at high frequencies with lower corner frequencies for long channel devices.



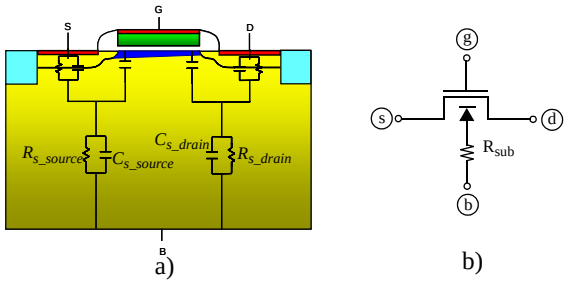
a) C_{gs} b) C_{gd}

Figure 3: Simulated a) C_{gs} and b) C_{gd} at 6.5 GHz and 17 GHz for L = 1.2 um for all bias region. In saturation region (i.e. V_{DS} = V_{GS} = 3 V) the degradation of C_{gs} between 2 frequencies is higher compared to C_{gd}, while the degradation of the C_{gs} and C_{gd} is similar in linear region.



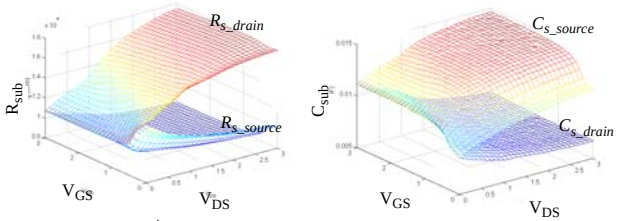
a) b)

Figure 4: a) when V_{DS} = V_{SS} = 0 and V_{GS} > V_{th}, inversion charge splits equally between drain and source resulting in L_{eff_gs} = L_{eff_gd}, b) V_{DS} > V_{SS} and V_{GS} > V_{th}, source side shares most of charge resulting in L_{eff_gs} > L_{eff_gd}.



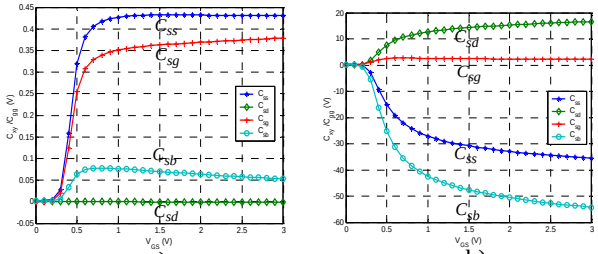
a) b)

Figure 5: a) substrate network of MOSFET and, b) simplified substrate network of MOSFET.



a) b)

Figure 6: Extracted substrate parameters of a) R_{sub} b) C_{sub}.



a) b)

Figure 7: Simulated C_{ss}, C_{sg}, C_{sd}, and C_{sb} at 10 Hz , $V_{DS} = V_{GS} = 3$ V for a) L = 10 um device, and b) L = 0.3 um device.

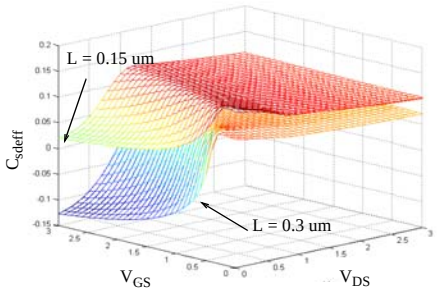


Figure 8: C_{sdeff} for L = 0.15um and L = 0.3um device at 10 GHz, where only intrinsic term, C_{sd}, remains. The C_{sd} becomes positive for shorter channel length (L=0.15 um) device.