SET Accurate Compact Model for SET-MOSFET Hybrid Circuit Simulation

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Abstract

Single-Electron Transistors (SETs) [1][2] are attractive candidates for post-CMOS VLSI ICs. Accurate models are also required in order to efficiently design SET circuits and hybrid circuits. We have developed a new physical compact model of SET [3][4], which enables the accurate simulation of SET circuits and hybrid circuits in a SPICE-like environment. We show advanced examples of applications of our approach: simulations of elementary circuits which functionalities have been experimentally demonstrated in the literature [5][6].

1 Introduction

SETs have attracted much attention because of their low power consumption and small size [1][2][7]. Recent works [5][6] show that Single-Electron Transistors could enable innovative functionalities if they are associated with MOSFETs. However Monte-Carlo (MC) simulation [8] is not adapted to the analysis and the optimization of realistic logic circuits with a large number of devices (MOSFETs and SETs).
In this paper, we propose a compact physically based SET model, describing SET characteristics accurately over a wide range of temperature and voltages [4]. Our approach is simpler and more efficient than those presented in the literature [9][10]. Our model has been validated in static and dynamic regimes [4], at both device and logic circuit levels, by comparison with the MC simulator SIMON [8].

2 SET modeling

Our model is derived on the basis of the "orthodox" theory of single charge tunnelling and the master equation method [1][2]. The number of elementary charges e in the SET island (Figure 1.a) is supposed to be n = -1, 0 or +1. This model (detailed elsewhere [4]) is built on this assumption and the periodicity of the current $I_{DS}(V_{GS})$: the average I_{DS} current (Figure 2.b) is determined as a function of the V_{DS} and V_{GS} voltage, the temperature and the offset charges, q_0.
We have checked that, in the dynamic or static regime, the difference between our model and MC simulation (Figure 2) is less that 1.5% for $|V_{DS}| \leq 2e/C_\Sigma$ ($C_\Sigma = C_1 + C_2 + C_G$ is the total capacitance of the central island), which is two times the limit of

the models proposed by Uchida [9] or Mahapatra [10]). We have checked that this result does not depend on the SET parameters (capacitances, resistances) and is validated for a large range of temperature ($kT / E_C < 0.1$).

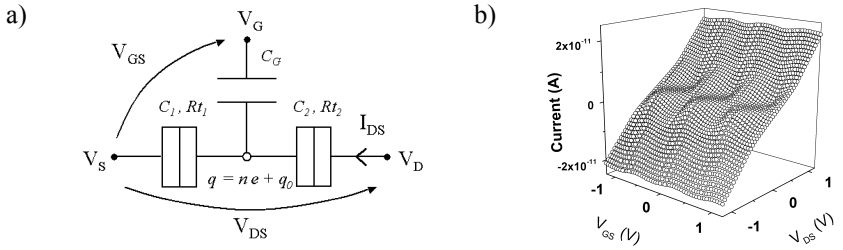

Figure 1: a) Schematic representation of a Single-Electron Transistor. b) Example of current I_{DS} calculated with our model. The blockade regions (diamond shape) can be clearly distinguished.

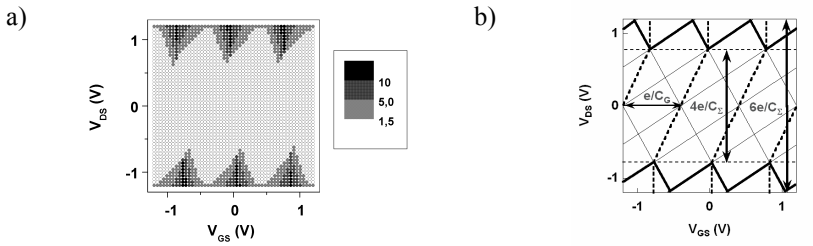

Figure 2: a) Example of relative error (%) between MC simulation and our model in the V_{DS}-V_{GS} diagram. In the central region the accuracy is better than 1.5%. b) Theoretical limits of validity of our model (which correspond to the MC results).

3 Applications to hybrid MOSFET-SET simulation

3.1 Ring oscillator with SETs

The first logic gates that we have simulated with our model (in SmarSpice with Verilog-A [11]) are ring oscillators composed of 2p+1 SET inverters [11] (Figure 3).

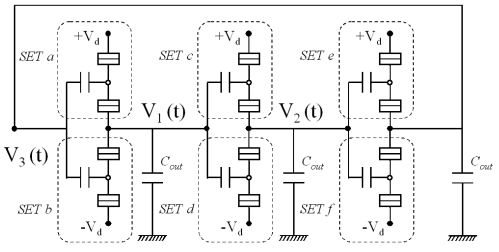

Figure 3: Ring oscillator with 3 SET inverters.

The voltages V_1, V_2 and V3 are the outputs of the 3 inverters. The supply voltages are $+V_D$ and $-V_d$. This circuit generates oscillating signals like in the case of CMOS inverters. Figure 4 shows the voltages of the outputs of the three inverters as a function of time, obtained by a Smartspice simulation [11]. This proves that our model allows to simulate this oscillating behaviour.

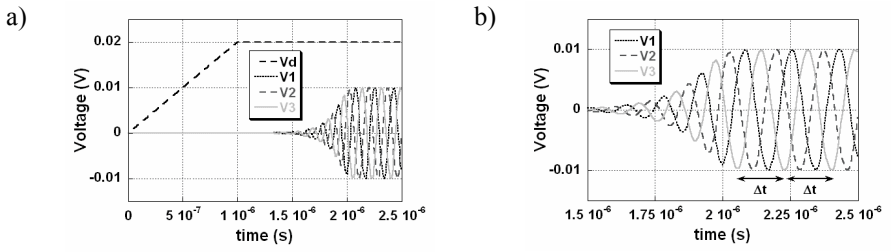

Figure 4: Simulation of the ring oscillator behaviour. When the supply voltage V_d is increased to its nominal value, the outputs voltages Vi oscillate (b : zoom of Figure a).

3.2 Hybrid SET-MOSFET circuits

We have also simulated the electrical behaviour of two hybrid MOSFET-SET circuits: a SRAM cell [5] and a "quantizer" [6] (Figure 5) proposed by Inokawa.

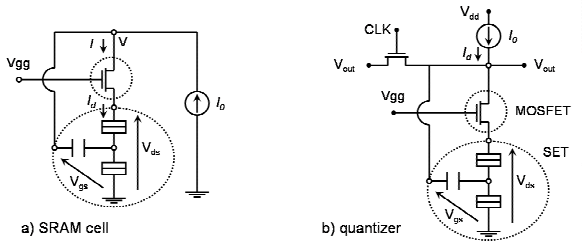

Figure 5: Schematic circuits proposed by Inokawa a) SRAM cell [5] (the multiple-value memory effect is due to the V-I hysteresis). b) "quantizer" [6] (the signal V_{in} is sampled with respect to the frequency defined by the "Clock" MOSFET along the stability points a, b, …, f).

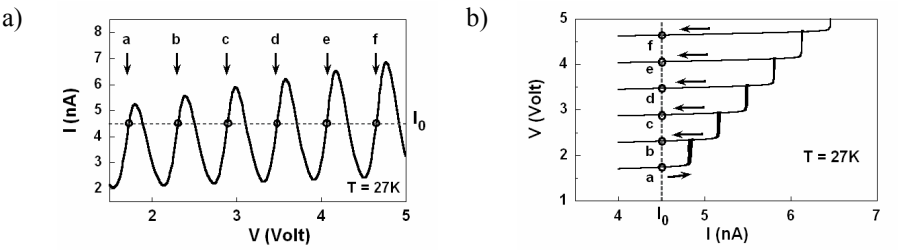

Figure 6: a) Current characteristic I(V) of the sub-circuit of the SRAM cell calculated by hybrid SPICE simulation. b) Multivalued hysteresis effect of the SRAM cell simulated by our model.

For most simulation parameters, we have considered the values extracted by Inokawa from measurements. We have used the following values: MOSFET: L = 14µm / W = 12µm / T_{ox} = 9.45nm - SET : C_J = 1.8aF / C_G = 0.07aF / Rt = 150kΩ / q_0 = e/2 / Vgg = 1.04V[5].
The simulated results (Figure 6 and Figure 7) show a very good agreement with these experimental measurements [5][6].

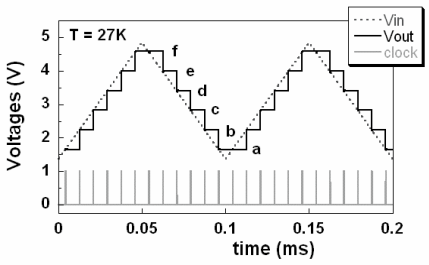

Figure 7: Simulation of the quantizer operation. The output voltage V_{out} (with a staircase shape with respect to the stability points) corresponds to the sampling of the triangular voltage V_{in}.

4 Conclusions

In this paper we propose a new compact model for SET dedicated to SPICE simulation for SET circuits and hybrid MOSFET-SET circuits. After showing the performances of our model, we apply it to the simulation of SET Logic gates and hybrid MOSFET-SET circuits. We demonstrate the accuracy of our model by the good comparisons between the SPICE simulations and the experimental measurements of these circuits [5][6].

Acknowledgment

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