2D Quantum Mechanical (QM) Charge Model and Its Application to Ballistic Transport of Sub-50nm Bulk Silicon MOSFETs

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Abstract

We consider the quantum mechanical (QM) effects along the channel in decanano-scaled MOSFETs and propose a novel approach to modeling the effect of tunneling current on the charge distribution in the carrier confinement dimension. Together with a QM correction in the poly gate region, the new analytical expression accurately predicts the surface charge density at the peak of the source-end potential barrier, which is a key parameter in the ballistic MOS compact model. The MOS model (called BMM and B for ballistic) thus developed has been proved to accurate through comparison to the experimental data of a 45nm MOSFET from TSMC [1]. Furthermore, the scalability of this model proves its robustness for ultra-small MOSFETs.

1 Ballistic MOS Model and Surface Charge Density

It has been proposed by Natori [2] and Lundstrom [3] that for ballistic-transport dominant MOS device, the drain current can be expressed as

$$\frac{I_D}{W} = Q(0)\frac{1-r}{1+r}\left[\upsilon_T \frac{\Im_{1/2}(\eta)}{\Im_0(\eta)}\right]\left(1-\frac{\Im_{1/2}(\eta-U_D)}{\Im_{1/2}(\eta)}\right)\Big/\left(1+\frac{1-r}{1+r}\frac{\Im_0(\eta-U_D)}{\Im_0(\eta)}\right) \tag{1}$$

where all notations can be found in [3]. Using the threshold voltage based approach with 1D quantum correction in the carrier confinement dimension (i.e., normal to the channel) the surface carrier density at $x_{\max}$ (position for the peak of the source-end potential barrier) is evaluated as $Q(0)=C_{ox}V_{\text{geff}}$ where

$$V_{\text{geff}} = 2\eta_0 V_T \ln\left(1+\exp\left(\frac{V_{\text{od}}}{2\eta_0 V_T}\right)\right)\Big/\left(1+2\eta_0 C_{ox}\sqrt{\frac{2\phi_{sqm0}}{q\varepsilon_{si}N_{sub}}}\exp\left(\frac{V_{\text{od}}-2(V_{GS}-V_{\text{th}}-V_{\text{off}})}{2\eta_0 V_T}\right)\right) \tag{2}$$

where all notations can be found in [4]. However, $Q(0)$ thus obtained tends to underestimate the surface carrier density for two reasons:

1. Neglect the QM effects in the poly gate, which result in a dipole with polarity in favor of threshold voltage reduction [5].
2. Like the graduate channel approximation (GCA) no longer applies to short channel devices, QM effects along the channel inevitably alter the 1D QM corrections in the carrier confinement dimension.

These phenomena have never been modeled in a physics-based, analytical way and we propose a novel approach to resolving these issues.

2.1 Correction to Threshold Voltage due to Lateral QM Effects along Channel

The key to our modeling is the realization that the tunneling through the source/drain (S/D) potential barrier along the channel not only adds to the drain current, but also lowers the ground energy level in the quantum well in the perpendicular direction to the channel. In 1D QM correction, $E_{\max}$ is taken as the edge of the 1st subband at $x_{\max}$. Considering the tunneling through S/D barrier, the energy corresponding to the lowest nonlocal, current-carrying eigenstate should be solved from the following relationship

$$\frac{i}{\hbar}\int_a^b \sqrt{2m_x[E'_{\max} - E_n^1(x)]}dx = -\alpha \tag{3}$$

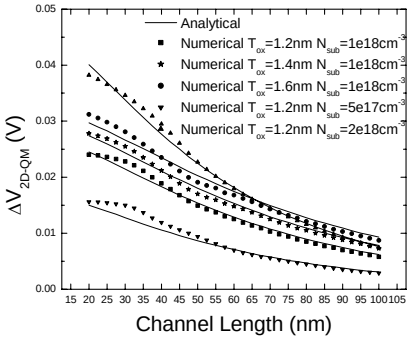
where $e^{-\alpha} << 1$ and in our case $\alpha = 4$, $E_n^1(x)$ is the profile of the 1st subband edge along the channel, and *a* and *b* are classical turning points in WKB theory and depend on $E'_{\max}$ and $E_n^1(x)$. Solving Eq. (3) numerically for $E'_{\max}$ and one obtains the correction to V_{th} as $\Delta V_{\text{th, 2Dqm}} = \left(E_{\max} - E'_{\max}\right)/q$. To avoid numerical solution, an analytical formula is proposed by approximating $E_n^1(x)$ as the parabola in the vicinity of $x_{\max}$ and introducing a parameter σ as the curvature of the parabola. Thus

$$\Delta V_{\text{th,2Dqm}} = -\frac{8\hbar}{q\pi}\sqrt{\sigma/2m_x}\left(1+\sqrt{\varepsilon_{si}q^2N_{sub}/k_BT\ln\left(N_{sub}/n_i\right)}/2C_{ox}\right) \tag{4}$$

where all symbols have conventional meaning. The analytical form for σ is further determined based on the analytical solution to 2D Poisson equation [6] as follows where all the notations can be found in [6]

$$\sigma = \left\{\left(V_{DS}+V_{bi}-\phi_S\right)\sinh\left(x_{\max}/l\right)+\left(V_{bi}-\phi_S\right)\sinh\left[\left(L-x_{\max}\right)/l\right]\right\}/\left[l^2\sinh\left(L/l\right)\right] \tag{5}$$

In Fig. 1 (a), $\Delta V_{\text{th,2Dqm}}$ from Eqs. (4) and Eq. (5) versus L is plotted with different T_{ox} and N_{sub}. The agreement between analytical and numerical results is acceptable. In Fig. 1(b), the analytical surface carrier densities are compared to the numerical simulations with different device parameters to prove the accuracy of this model (error below 3%). It can be seen that without $\Delta V_{\text{th,2Dqm}}$, the errors are evident.



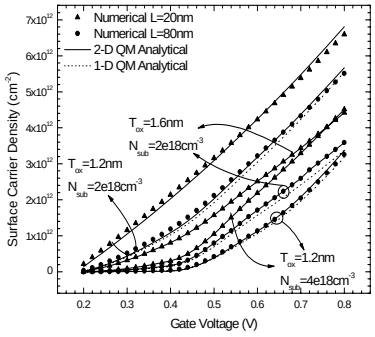


Figure 1 : (a) $\Delta V_{\text{th,2Dqm}}$ vs. L at $V_{DS} = 0$. (b) Surface carrier density vs. V_{GS}.

2.2 Semi-Empirical Model for QM Effects in Poly Gate

On top of classical poly-depletion (PD) in the poly gate is an electric dipole formed near the poly/gate-oxide interface due to QM effects [5]. These two effects have opposite influence on the effective gate biasing applied to the gate oxide and the substrate: PD reduces while QM in poly increases the biasing. The PD effects have been modeled in previous works while the QM in poly is modeled analytically for the first time in this work based on density gradient formulation [7]. The correction due to the QM in poly is finally established as follows

$$\Delta V_{\text{th,PGqm}} = \frac{C_{ox}^2 \hbar^2 q}{8c1 k_B^2 T^2 m_h^* \varepsilon_{si}^2}\left(V_{GS} - V_{FB} - \phi_S + \frac{k_B T}{q} - \frac{4m_h^*(k_B T)^3 \varepsilon_{si}}{\hbar^2 q^3 N_p}\right)^2 + c2\left(\frac{k_B T}{q} + \frac{4m_h^*(k_B T)^3 \varepsilon_{si}}{\hbar^2 q^3 N_p}\right) \quad (6)$$

where N_p stands for the doping concentration in poly and $c1$ and $c2$ are fitting parameters that are related to N_p and T_{ox}. In Fig. 2 (a), the model results are compared to the numerical simulated results with an average error lower than 3%. It is seen that the QM in poly causes a threshold voltage reduction and a gate capacitance shift. In Fig. 2 (b), it is shown that the heavier the poly region is doped, the more acute the QM effects are.

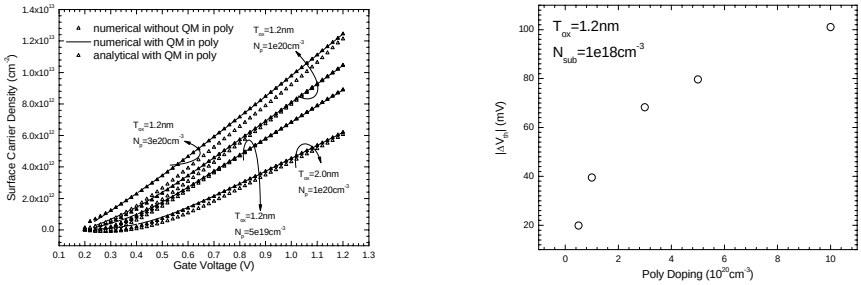


Figure 2 : (a) Surface carrier density with different N_p and T_{ox}. $N_{sub} = 1\text{e}18\text{cm}^{-3}$. (b) $\Delta V_{\text{th,PGqm}}$ versus poly-gate doping.

2.3 Compact I-V Model

After establishment of models for QM effects, short channel effects (SCE) and drain induced barrier lowering (DIBL) are further included and a compact *I-V* model, BMM, is completed with following threshold voltage expression

$$V_{\text{th}} = V_{\text{th,1Dqm}} + \Delta V_{\text{th,2Dqm}} + \Delta V_{\text{th,PGqm}} + \Delta V_{\text{th,SCE}} + \Delta V_{\text{th,DIBL}} \quad (7)$$

With $V_{\text{th,1Dqm}}$ represents 1D-QM corrected V_{th} as is done in [4].

3 Results and Analysis

To test this model, the analytical results and the experimental data of a sample device, fabricated by TSMC using the 90nm technology node with the channel length L of 45nm [1], are analyzed. The nitrided-silicon-dioxide is used as the gate-dielectric with the EOT of 1.3nm. The halo implant and the SSRC technology are used, making the channel highly non-uniformly doped, with an average doping of $1.25\text{e}18\text{cm}^{-3}$. In Fig. 3 (a), the comparison of the output characteristics between experimental data and analytical results is shown. It is clear from Fig. 3 (a) that with $\Delta V_{\text{th,2Dqm}}$, the results are satisfactory (error around 3%), while without it, the analytical results underestimate the drain current (error larger than 10%), indicating that mere 1D QM corrections in the transverse direction over-predict the increase of V_{th} due to overall QM effects. Furthermore, an improved mobility model and its parameter extraction strategy have been developed and the scalability is further tested using three groups of sub-100nm devices using QDD numerical simulation [7]. The results are shown in Fig. 3 (b).

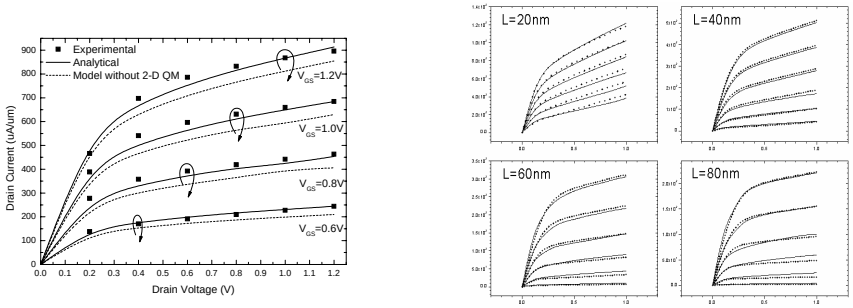


Figure 3 : (a) Output characteristics of the 45nm n-MOSFET from TSMC [1]. (b) Test of scalability. Dash lines are numerical results and solid lines are from BMM.

4 Conclusion

Proper modeling of QM effects along channel are indispensable for the predictability of MOS compact model. Combined with ballistic transport, a BMM model has been developed to accurately analyze the *I-V* characteristics of sub-50nm MOSFETs.

References

[1] TSMC 45nm MOSFET, internal documentation.

[2] K. Natori, *IEICE Tr. Electron.*, Vol. E84-C, No. 8, pp. 1029-1036, Aug. 2001.

[3] A. Rahman and S. Lundstrom, *IEEE Tr. Electron Devices*, vol.49, pp.481-489, Mar. 2002.

[4] Y. Ma, *et al.*, *IEEE Tr. Computer-Aided-Design of Integrated Circuits and Systems*, Vol. 20, No. 4, pp. 495-502, 2001.

[5] A. Svizhenko, *et al.*, *Journal of Applied Physics*, Vol. 91, No. 4, pp. 2343-2354, Feb. 2002.

[6] Z. Liu, *et al.*, *IEEE Tr. Electron Devices*, Vol. 40, No. 1, pp. 86,Jan. 1993.

[7] Z. Yu, *et al.*, *SISPAD*, p.1, Athens, Greece, Sept. 2001.