Modeling of Stress Induced Layout Effect on Electrical Characteristics of Advanced MOSFETs

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Abstract

Layout dependent stress induced effects on current drivability of 90nm node CMOS devices have been modeled by both performing stress modeling in process simulation and device simulation with stress dependent mobility model. It has been demonstrated that dependence of drive current of both n- and p-MOSFETs on source/drain size is successfully modeled. In addition, with this procedure, the performance improvement with stress engineering such as modifying shallow trench isolation (STI) process and using nitride liner deposition on gate electrodes can be well reproduced.

1 Introduction

Stress engineering has become one of the key issues for advanced CMOS technology because the performance improvement by carrier mobility enhancement with strain is significant. Recently, for the performance enhancement, novel schemes such as using buried SiGe layer in source/drain [1] and, SiN liner on gate electrode [2] have been reported. The strain, however, is pattern dependent. In addition, the strain itself is hard to monitor. Thus, for introducing stress engineering into the manufacturing process, the calibrated models for studying the impact of stress by TCAD simulation are indispensable.

In this paper, we have modeled the impact of stress on the current drivability of MOSFETs such as its dependence on active area size. 2D stress analysis based on process simulation has been performed, and its output of strain is used as the input of stress dependent mobility model in device simulation. With this scheme, the layout dependence of the drain current I_d of MOSFET such as source/drain size L_{sd} has been well predicted. Finally, the improvement of I_d has been simulated successfully when applying stress engineering such as embedding SiN liner layer in STI and using SiN capping layer on the gate electrode.

2 Experimental & Simulation Setup

MOSFETs used in this study were fabricated with 90nm node bulk CMOS technology. Gate oxide thickness is 1.8nm and gate length is 70nm. The layout of the test pattern is shown in Fig.1. L_{sd} is varied in the range from 0.24μm to 2μm. MOSFETs with different L_{sd} have been characterized. It is expected that with

decreasing L_{sd}, compressive uniaxial stress in the MOSFETs is increased due to the presence of STI as shown in Fig.2.

The simulation flow used in this study is schematically shown in the Fig. 3. ISE DIOS has been used as process simulator whose diffusion parameter set has been calibrated beforehand. Two sets of process simulation, one for doping profiles, and the other for stress have been carried out because a different mesh is suitable for stress and doping profile simulation. At the process of re-meshing for device simulation, the information of internal stress and doping profiles has been merged.

ISE Dessis has been used as device simulator. A piezo-resistive approach has been used for nMOSFET with piezo resistance parameter after Kanda [3]. For pMOSFET, the mobility modulation model based on deformation potential theory is used [4]. In this model, with the band-splitting due to strain, the redistribution of holes between heavy-hole band and light-hole band leads the change of the hole mobility.

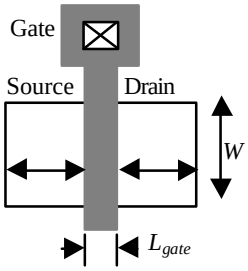

Figure 1: MOSFET test pattern for layout dependence analysis. L_{sd} is varied in the range from 0.24μm to 2μm.

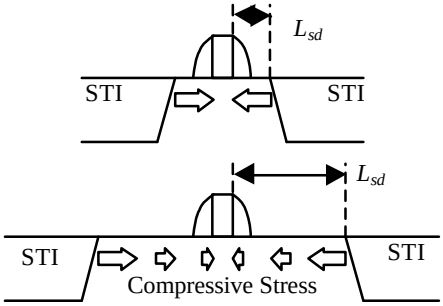

Figure 2: Schematic illustration of channel region stress. Compressive stress is large in small L_{sd}.

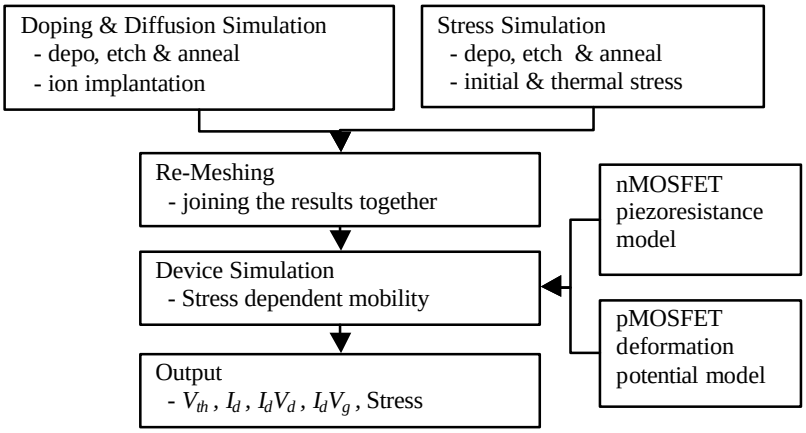

Figure 3: Simulation flow. Doping & diffusion simulation and stress simulation have been carried out, separately.

3 Result and Discussion

The simulated stress distribution around gate electrode is shown in Fig.4. Though STI creates large compressive stress near its vicinity, the channel region stress is tensile as shown in Fig.4 (a) and (b). It is because SiN layer around the gate has highly tensile initial stress exceeding 1GPa. The channel region stress decreases with reducing L_{sd}. It reaches +60MPa at L_{sd} of 0.24μm.

In Fig.5, the dependence of L_{sd} on I_d is shown for both n- and p-MOSFET with L_{gate}=70nm. For nMOSFET, I_d decreases when L_{sd} is reduced. I_d with L_{sd}=0.24μm is about 19% lower than that with L_{sd}= 2μm in the experiment. On the contrary, for pMOSFET, I_d increases when L_{sd} is reduced. I_d with L_{sd}=0.24μm is about 6.2% higher than that with L_{sd}= 2μm in the experiment. This tendency on L_{sd} is well described in the simulation. It is explained by the change of stress in the channel region with L_{sd} as the relation between stress S_{xx} and I_d of the nMOSFET is shown in Fig.6.

L_{sd} dependence of V_{th} is shown in Fig.7. There is small V_{th} shift in this case, which indicates that the neglect of stress effect on doping diffusion can be justified.

Finally, the impact of process induced stress is modeled. The effect of SiN liner around the gate electrode and the inclusion of SiN liner layer in STI have been simulated and compared with the experiment. Due to tensile stress of nitride layer, I_d can be increased by canceling the STI induced compressive stress in these structures as shown in Fig. 8.

Table 1 summarizes the simulated results of the stress induced effect on the change of I_d of nMOSFET. It has been demonstrated that the experimental results is well described by the simulation. The experimental I_d increase of 7% by both increasing SiN layer thickness and initial stress is well described by the simulation as shown in Table.1. In addition, the effect of SiN layer in STI is also well predicted as the simulated I_d increase of 4% is in good agreement with the experiment.

These facts indicate that the proposed modeling can be used for optimizing and investigating the stress effect on electrical characteristics of advanced MOSFETs.

4 Conclusion

Stress induced layout effect on electrical characteristics of 90nm node MOSFETs has been modeled successfully to give the good agreement with the experimental results. It has been shown that these methodologies can be used as an optimization tool for the stress control in future CMOS technology.

Acknowledgment

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References

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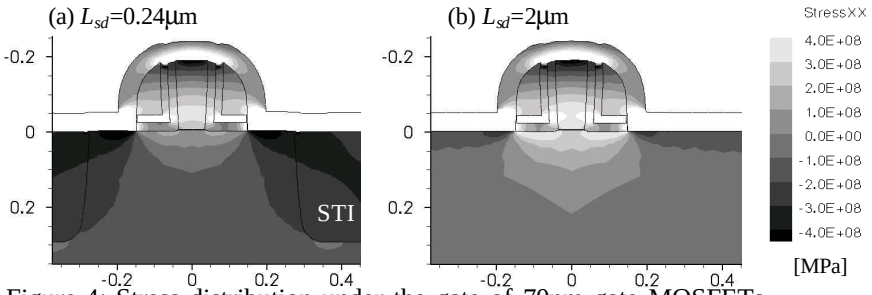

Figure 4: Stress distribution under the gate of 70nm gate MOSFETs with L_{sd}=0.24 μm (a) and L_{sd} = 2μm (b).

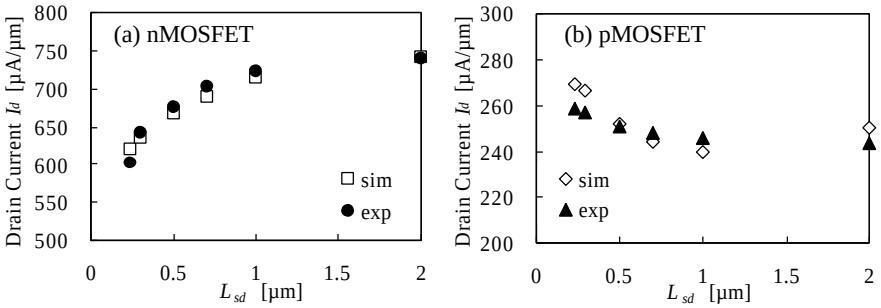

Figure 5: Relation of L_{sd} and I_d for nMOSFET (a) and pMOSFET (b). The simulation is in agreement with the experiment.

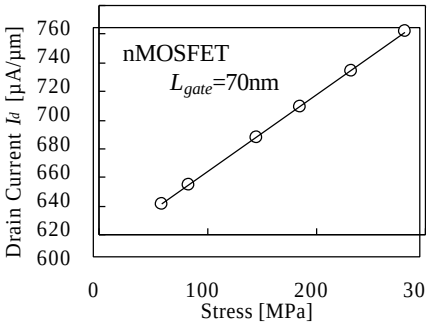

Figure 6: Relationship of I_d and the channel region stress.

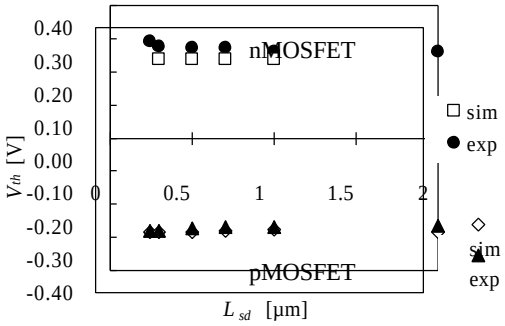

Figure 7: Dependence of V_{th} on L_{sd}.

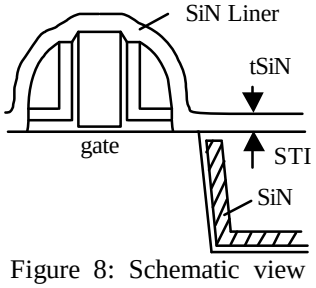

Figure 8: Schematic view of stress induced structure.

	initial stress	tSiN	sim. d I_d%	exp. d I_d%
SiN Liner	ref	ref	---	---
	1.5*ref	ref	+3.6	+4.0
	1.5*ref	1.5*ref	+6.7	+7.0
SiN in STI	without		---	---
	with		+3.8	+4.0

Table 1: Comparison of simulation with the experiment on I_d improvement of nMOSFET by mechanical stress enhancement.