A Monte-Carlo Method for Distribution of Standby Currents and its Application to DRAM Retention Time

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Abstract

We propose an efficient and accurate simulation method to predict the distribution of the standby currents. The leakage currents caused by the trap-assisted and band-to-band tunneling are evaluated from the current Green's function and cell-to-cell variations of traps and electric field are generated by Monte-Carlo (MC) method. We apply our method to obtain the retention time distribution of DRAM cell transistors and simulation results show the main and tail parts of the data retention time distribution and their temperature and bias dependences clearly.

1 Introduction

The failure in the data retention and the increase in the standby power caused by the junction leakage are the major reliability issues for realizing low power and high density memory and logic chips. The leakage current is determined by the several kinds of leakage sources. Amomg them, the Shockley-Read-Hall process enhanced by the trap-assisted tunneling (TAT) can give rise to large device-to-device variation of the leakage current since its magnitude is very sensitive to the trap energy level and the local electric field [1].
In the present paper, we introduce an efficient and accurate method to obtain the leakage current distribution and applied our method to determine the retention time distribution of DRAM cell transistors. We will also explain the possible origin of the tail distribution found in the DRAM chips.

2 Basic Models

The data retention time of a DRAM cell can be expressed as [2]

$$T_{\mathrm{RET}} = \left\{ C_{\mathrm{S}} \left(V_{\mathrm{CC}}/2 - \Delta V_{\mathrm{BL}} \right) - C_{\mathrm{BL}} \Delta V_{\mathrm{BL}} \right\} / I_{\mathrm{L}} \tag{1}$$

where C_{S} and C_{BL} are the storage and the bitline capacitances, V_{CC} is the supply voltage, and ΔV_{BL} is the bitline sensing voltage. I_{L} is the total leakage current that consists of the channel current (I_{CH}) due to punch through, the diffusion current (I_{DIF}), the TAT current (I_{TAT}), and the band-to-band tunneling (BBT) current (I_{BBT}) as

$$I_{\mathrm{L}} = I_{\mathrm{CH}} + I_{\mathrm{DIF}} + I_{\mathrm{TAT}} + I_{\mathrm{BBT}}. \tag{2}$$

Since the generation currents due to TAT and BBT are small enough for the bias conditions of interest, these currents do not disturb the DC solution significantly. Therefore,

I_{CH} and I_{DIF} can be precalculated at the first stage of the simulation. The remaining terms in (2) can be obtained by superposing all the carrier generation sources weighted by the current Green's functions under the assumption that the drain current response due to the generation sources are linear. Therefore, the TAT current by N traps located at $\{\mathbf{r}_{\mathrm{j}}\}$ with their energy levels $\{E_{\mathrm{j}}\}$ (relative to the intrinsic level) can be written as

$$I_{\mathrm{TAT}} = -\sum_{\mathrm{j}=1}^{N} R_{\mathrm{trap}}\left(\mathbf{r}_{\mathrm{j}}, E_{\mathrm{j}}\right)\left\{G_{\mathrm{n}}\left(\mathbf{r}_{\mathrm{j}}\right) + G_{\mathrm{p}}\left(\mathbf{r}_{\mathrm{j}}\right)\right\}, \tag{3}$$

where G_{n} and G_{p} are the Green's functions of the electron and hole [3]. R_{trap} is the net recombination rate due to a single trap that depends on the electron density (n), the hole density (p), and the magnitude of the electric field (F) at $\mathbf{r}_{\mathrm{j}}$ as [4]

$$R_{\mathrm{trap}} = \frac{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}} v_{\mathrm{th}}\left(pn - n_{\mathrm{i}}^2\right)}{\frac{\sigma_{\mathrm{n}}}{1+\Gamma_{\mathrm{p}}}\left(n + n_{\mathrm{i}} e^{E_{\mathrm{j}}/k_{\mathrm{B}}T}\right) + \frac{\sigma_{\mathrm{p}}}{1+\Gamma_{\mathrm{n}}}\left(p + n_{\mathrm{i}} e^{-E_{\mathrm{j}}/k_{\mathrm{B}}T}\right)}, \tag{4}$$

where v_{th} (10^7 cm/sec) is the thermal velocity, $\sigma_{\mathrm{n,p}}$ are the capture cross sections, and $\Gamma_{\mathrm{n,p}}(F)$ are the field enhancement factors. To obtain accurate leakage current due to a trap at arbitrary position $\mathbf{r}_{\mathrm{j}}$, all the physical quantities are linearly interpolated using the values of adjacent nodes. The BBT current can be calculated similarly as

$$I_{\mathrm{BBT}}(F) = -\int_{\Omega} d\mathbf{r} R_{\mathrm{bbt}}\left(F\left(\mathbf{r}\right)\right)\left\{G_{\mathrm{n}}\left(\mathbf{r}\right) + G_{\mathrm{p}}\left(\mathbf{r}\right)\right\}, \tag{5}$$

where $-R_{\mathrm{bbt}}$ is the BBT generation rate and Ω is the whole simulation domain. We have compared the leakage current obtained from (2), (3), and (5) with the self-consistent DC simulation and confirmed that the two results are in good agreement. Therefore, once the Green's functions are obtained for the device under the given bias condition, the current fluctuation can be easily obtained by the MC technique with the random variables for the trap density, spatial distribution, trap energy. In this study, the effect of the electric field fluctuation is also considered by assuming that the electric field of each cell is distributed as

$$F\left(\mathbf{r}\right) = F_0\left(\mathbf{r}\right) \times (1 + f), \tag{6}$$

where F_0 is the electric field obtained from the DC solution and f is a Gaussian random variable whose mean and standard deviation are zero and σ_{F} respectively. The overall MC simulation procedure is outlined in Fig. 1.

3 Simulation Results and Discussion

We simulate the retention time distribution of a DRAM chip whose minimum feature size is $0.16\ \mu\mathrm{m}$ as shown in Fig. 2. The traps are treated as uniformly distributed in the $\mathrm{Si/SiO_2}$ interfaces adjacent to the gate-oxide and the shallow-trench isolation (STI). Fig. 3 shows the sum of the electron and the hole current Green's functions. The sum is maximum near the drain depletion region. Fig. 4 shows the I_{DIF}, I_{CH}, and $I_{\mathrm{BBT}}(F_0)$ with respect to the gate bias. If the field fluctuation is neglected, the sum of these three currents determines the upper limit of the retention time. Fig. 5 shows the temperature

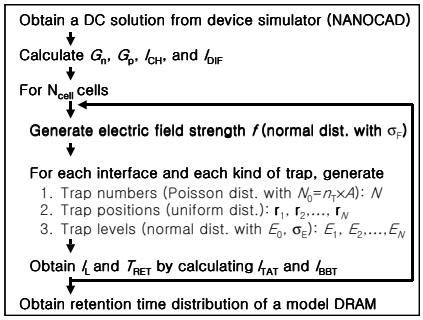

Figure 1: Flow of the Monte-Carlo method.

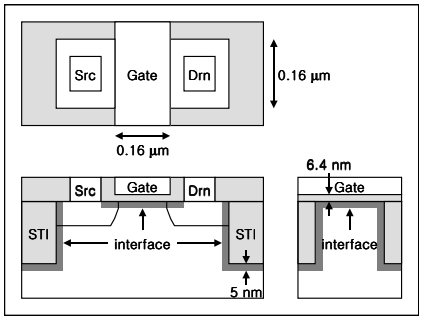

Figure 2: Structure of the DRAM cell transistor.

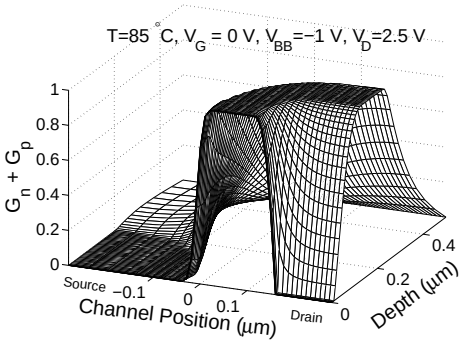

Figure 3: Sum of the current Green functions for electrons and holes.

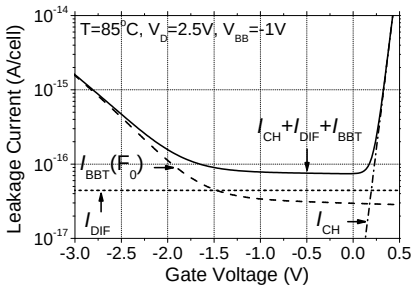

Figure 4: I_{DIF}, I_{CH}, and I_{BBT} (F_0) vs. gate voltage.

dependence of the retention time distribution. In the simulation, the effect of field fluctuation is neglected ($\sigma_{\mathrm{F}} = 0$), $\sigma_{\mathrm{n,p}}$ are 10^{-15} cm^2, the interface trap density (n_{T}) is 1.58×10^{10} cm^{-2}, the average trap level (E_0) and its standard deviation (σ_{E}) are -0.2 eV and 0.03 eV, respectively. We also simulate the effect of field fluctuation as shown in Fig. 6. As the field fluctuation is increased, the retention times of tail cells decrease. The bias dependences of the retention time distribution are shown in Fig. 7 and Fig. 8. As the gate bias increases negatively, the main and the tail distribution both broaden and the retention times of the tail cells decrease largely relative to the main cells. In the case of the well bias, the average retention time is reduced while the shape of the distribution is not changed significantly.

4 Conclusion

We studied the data retention time distribution of a DRAM chip by introducing the Green's function technique and the Monte-Carlo simulation. The tail cell is usually caused by a single trap at the high electric field region. We believe that our technique can be applied not only to the study of geometry, doping profile, and bias dependences of the retention time but also to the leakage current of the logic devices.

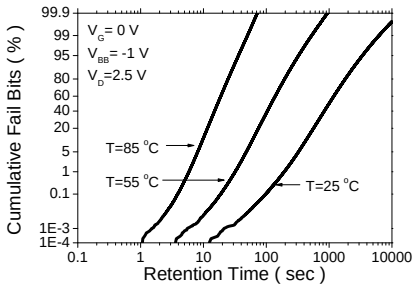

Figure 5: Temperature dependences of the retention time distribution.

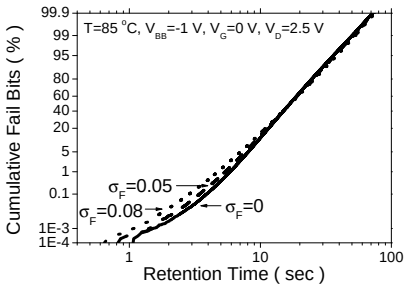

Figure 6: Effect of field fluctuation on the retention time distribution.

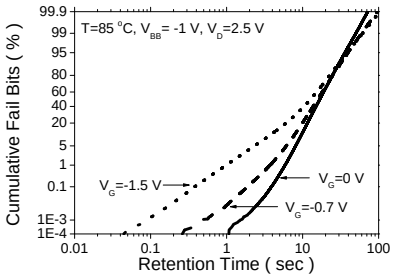

Figure 7: Gate bias dependence of the retention time distribution.

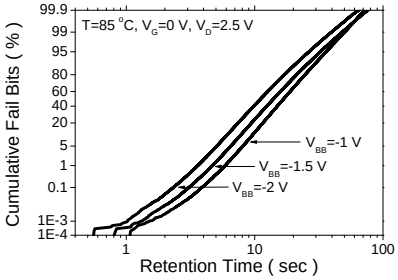

Figure 8: Well bias dependence of the retention time distribution.

Acknowledgment

This work was supported by the *National Research Laboratory Project of the Ministry of Science and Technology* and the *Nano Systems Institute - National Core Research Center (NSI-NCRC) program of KOSEF, Korea*.

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