Strain Scaling for Ultra Thin Silicon NMOS Devices

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Abstract

Ultra thin FDSOI devices with very high performance have been reported [1-2]. Strained silicon directly on insulator (SSDOI), and ultra thin germanium on insulator have been recently demonstrated with large amounts of strain in the thin active layer [3-4]. Using 3-d computer simulations, we show how the strain will scale down to the 32nm technology node. Due to on-going development efforts we limit our work to NMOS devices only. We investigate geometrical effects and process dependency. Our results show that significant performance enhancement will be possible by applying process-induced stress.

Strain design is an important device optimization process and significant performance enhancements have been reported using both uniformly strained layers as well as process induced strain [5-7]. Many processing steps relax the strained silicon layer. There are also interaction effects, induced by different layers with intrinsic stress. To compare SSDOI and unstrained ultra thin SOI devices with geometries down to 15nm, we use 3-d process and device simulations that take into account local stress tensor and its effect on local mobility [8] for NMOS ultra thin body devices. The 3-d process simulations use all thermal and process-induced steps we anticipate for a 45 or 32nm node technology.

1 Device Structure

A schematic of a generic device used in our simulations is shown in Fig.1. There is an ultra thin silicon layer over the buried oxide. The gate wraps around the channel from three sides due to mesa isolation. The channel lies on a pedestal, caused by over-etching of the buried oxide. Thickness of the gate oxynitride is 1.5nm, spacer is 20nm wide with default intrinsic stress of -100MPa. The selective epi layer is 20nm thick and fully converted into a silicide with default stress of 1GPa. A 50nm thick SiON layer is used for ILD planarization (default stress -100MPa), which can also serve as a stressed over-layer. In simulations, the gate is converted into a FUSI gate [1,9] (default stress 1GPa) as a gate last process. When measuring performance enhancements, we compare device simulations that use stress-dependent local mobility to device simulations with stress-dependence turned off, while keeping the same geometry and the same quantum effects.

2 Simulation Results

To gain an insight into 3-d stress effects we assign uniform stress components for all three dimensions for a 10nm thin silicon channel with L=25nm and W=50nm. Fig.2 shows linear transconductance enhancements, compared to a case without any stress. We see that there are cases where stress can degrade performance. We get the largest enhancement from large tensile longitudinal and transverse stresses, and compressive

perpendicular stresses. This result is similar to the 3-d stress recommendations for bulk devices [7]. Since the perpendicular component of stress is important we expect that there will be a need for a trade-off because holes favor the opposite sign of perpendicular stress [7]. The drive currents have larger enhancements, attributed to the lower V_t for devices with large compressive perpendicular stress (Fig.3). When we compare drive currents in the subsequent study, we take into account that process-induced strain can change threshold voltages.

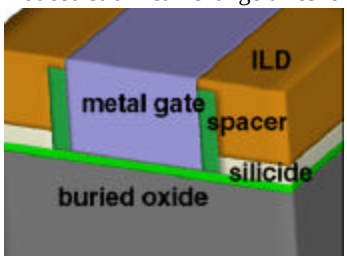

Fig.1: Structure of the ultra thin body device.

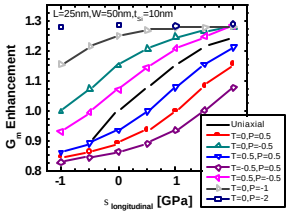

Fig.2: G_m enhancement for uniformly strained devices in transverse and perpendicular directions.

We use four different geometries that should mimic a representative variety of gate lengths and widths (for L=150nm we use W=250 and 25nm with silicon thickness 10nm; for L=15nm, we use W=250 and 25nm with silicon thickness 5nm). First, we study the effect of gate intrinsic stress, while keeping intrinsic stresses in other layers at the default value. From Fig.4 we see that SSDOI shows significant performance enhancement over non-strained SOI, using the default process-induced strain, for gate lengths down to 15nm. The largest drive current improvement is achieved by using a gate with compressive intrinsic stress. The enhancement increases with smaller gate length. For larger gates gate stress has different effect for different gate width. The strain in the silicon layer improves drive currents by 15-20%, depending on geometry (Fig.5). Narrow unstrained devices have larger currents [9] and strained silicon doesn't improve drive current that much.

The threshold voltage is also affected by quantum mechanical effects, which become dominant at thinner channel thickness. The higher occupancy of lower sub-bands can increase drive current [10]. We observe that there is also a stress benefit from thinner channels for shorter gate lengths (Fig.6). Thinner channels have higher tensile longitudinal and less tensile perpendicular strain. Fig.6 also shows that there is an optimal thickness for each gate length. Since strained silicon devices have different threshold voltages [3], we compare SSDOI and SOI devices for the same gate over-drive. Fig.7 shows that for 15nm devices, a 5nm thick channel gives the highest drive current and transconductance. Different stress in the thin spacer has little effect on devices with small L&W (Fig.8), but for larger widths the tensile stress is beneficial. A tensile ILD over-layer can improve drive current of unstrained devices by ~10%. There is a significant interaction between silicide stress and strain in the silicon layer and SSDOI devices prefer compressed silicide, while unstrained devices have better performance with tensile one. Thicker epitaxial layers provide thicker source/drain silicide layers and thus improve performance. While this is beneficial for DC, it may be detrimental for AC performance. If we move epi and silicide out with a thicker spacer (40nm), increased R_{sd} compensates all stress-induced improvements, thus making epi thickness a less desirable strain design knob. The optimal stress for both SSDOI and

SOI is shown in Table 1. Further optimization is necessary since 3-d stress effects are coupled. I-V curves for optimal SSDOI and SOI 25nm devices are shown in Fig.9. The SSDOI device with the strained silicon layer shows marginal improvement for larger drain voltage. The pedestal height showed effects on drive current [11]. Larger pedestals have higher threshold voltages and for the same gate overdrive it has very little effect on drive current (Fig.10). Instead of silicon growth one can grow SiGe [5], but for ultra thin NMOS SSDOI devices this degrades G_m (Fig.11).

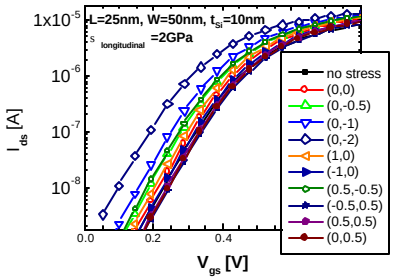

Fig.3: I-V curves for different uniformly strained devices (first number-transverse, second number-perpendicular, in GPa).

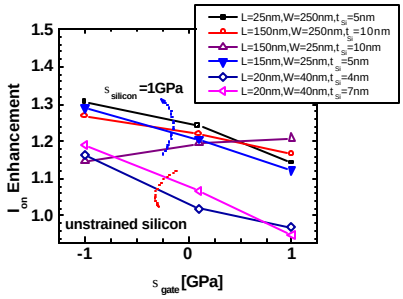

Fig.4: Drive current enhancement for different intrinsic gate stress.

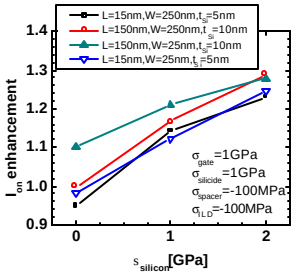

Fig.5: Drive current enhancement for different silicon stress.

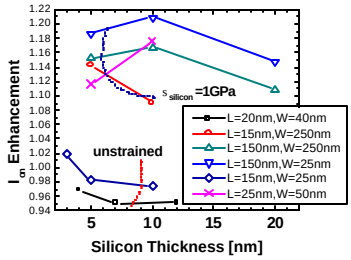

Fig.6: Silicon thickness effect on drive current enhancement.

4. Conclusions

Computer simulations show that ultra thin SSDOI and FDSOI devices benefit from compressive gate and tensile spacer and ILD layers. The silicide stress has different effects on strained and unstrained devices. Compressive silicide benefits SSDOI, while tensile silicide benefits SOI devices. With optimal process-induced stress we expect only marginally better performance enhancements for SSDOI NMOS devices for the 32nm technology node.

References

[1] J. Kedzierski et al, IEDM 2003, pp.441
[2] Z. Krivokapic et al, SSDM 2003, pp.760
[3] K. Rim et al, IEDM 2003, pp.49
[4] S. Takagi et al, IEDM 2003, pp.57
[5] T. Ghani et al, IEDM 2003, pp.978
[6] F-L Yang et al, IEDM 2003, pp.627
[7] C.H. Ge et al, IEDM 2003, pp.73

[8] V. Moroz et al, *Materials Science in Sem. Proc.*, **6,** p.27-36,2003
[9] Z. Krivokapic et al, IEDM 2002, pp. 271
[10] S. Takagi, VLSI Symp. 2003, pp.115
[11] Z. Krivokapic et al, IEDM 2003, pp.445

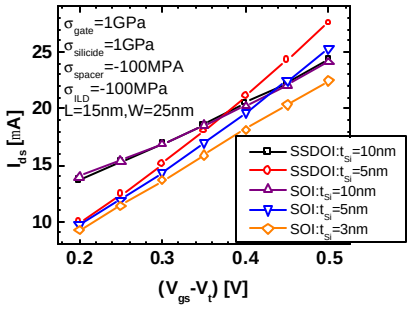

Fig.7: I_{ds} for a 15nm device with different silicon channel thickness.

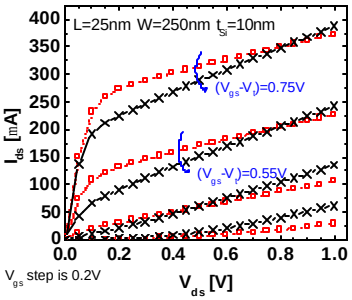

Fig.9: I-V curves for optimal process-induced stress in SSDOI (cross) and SOI (square).

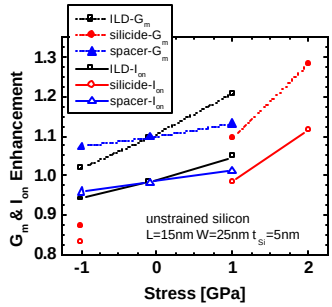

Fig.8: I_{on} and G_m enhancements for different stress in ILD, spacer, and silicide.

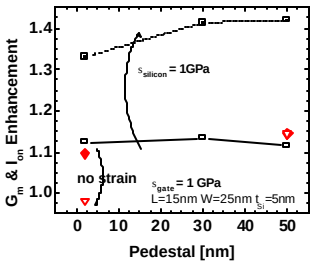

Fig.10: Performance enhancement dependence on pedestal height.

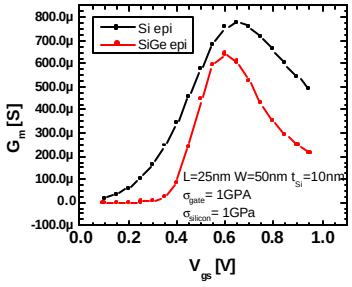

Fig.11: Si and SiGe epi for 25nm SSDOI devices.

Layer	SSDOI	SOI
gate	compr.	compr.
silicide	compr.	tensile
spacer	tensile	tensile
over-layer	tensile	tensile

Table 1: Optimal process-induced stress for SSDOI and SOI devices