Implications of Gate Misalignment for Ultra-narrow Multi-gate Devices

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Abstract

Multi-gate devices rely on a very thin body to achieve good electrostatic control. While narrow channel is desirable, narrow source/drain extensions can increase parasitic capacitance. Different layout approaches (tapered source/drain, dog-bone transistor) have been used to alleviate this problem, resulting in quite different currents [1]. Multi-gate devices with L=20nm and W=65nm and excellent device performance were reported [2]. An important aspect of their manufacturability is how important the misalignment of the gate relative to the source and drain is. In this paper we present experimental and simulation data for the 45nm technology node and present interesting results for variable-width transistors.

1 Device Structure

An aerial image simulation result for a four-finger narrow transistor is shown in Fig.1. An evolutionary 193nm lithography tool with dipole illumination will be able to print 130nm pitch required for the 45nm technology node. A lithographic result is a funnel-like channel with the thinnest channel width in the middle. By importing the channel shape from Fig.1 into 3D Taurus Process simulator we build devices with different degrees of gate misalignment (Fig.2). A generic device used in our simulations has an ultra thin silicon layer over the buried oxide. The gate wraps around the channel from three sides due to mesa isolation. The channel lies on a pedestal, caused by over-etching of the buried oxide. Gate oxynitride thickness is 1.5nm; spacer is 20nm wide with built-in compressive intrinsic stress of 100MPa as is the stressed over-layer. The metal gate has a tensile intrinsic stress of 1GPa.

2 Experimental Data

Measuring available test structures (L=25nm, W=60nm, t_{Si}=9nm) we found out, that devices with gate misalignment of 25nm toward drain have smaller off-state leakage and larger drive current (Fig.3). Such devices have variable width; width on the source side of the transistor is smaller than on the drain side. The peak linear transconductance, which is a measure of carrier mobility, is also larger for the misaligned device (Fig.4).

3 Simulation Results

Process simulations take into account stress history during all thermal steps and intrinsic stresses of all layers as described in [3]. Doping profiles are constructed based

on analytic 3D distributions due to the lack of diffusion models in ultra-thin silicon layers in the presence of GPa-scale highly anisotropic strain. Components of the stress tensor are used to calculate local mobility for each grid point [3]. For quantum mechanical corrections we use the Modified Local Density Approximation [4], but surface roughness effects for very thin silicon films are neglected. The channel is undoped, and we define L_{eff} as the distance between the source and drain (at electron concentrations of 10^{16} cm^{-3}).

The process-induced stress affects band structure as shown in Fig.5. While for centered gates the conduction band is symmetric, the geometrical effects of process-induced stress cause asymmetry for misaligned gates, lowering the source-to-channel barrier (Fig.5). In our simulations we first study NMOS devices with L=20nm, W=45nm, and silicon thickness of 10nm. A mid-gap gate work function is assumed.

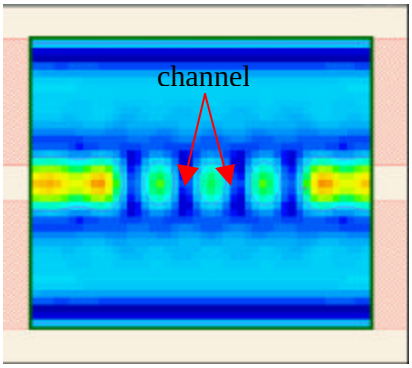

Fig.1: Aerial image of multi-finger 45nm wide multi-gate device.

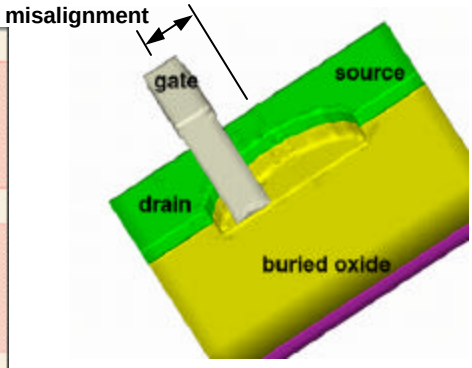

Fig.2: Half width of a 45nm narrow transistor with 25nm misalignment.

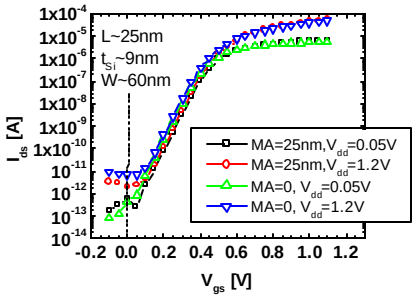

Fig.3: Experimental transfer characteristics for L=25nm narrow devices with deliberate gate misalignment of 25nm toward the drain.

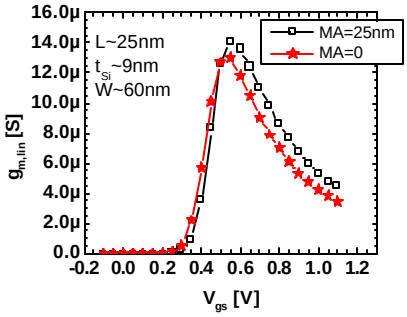

Fig.4: Measured $g_{m,lin}$ for 25nm narrow devices with deliberate gate misalignment.

The channel thickness is too large to achieve an acceptable I_{off} for the centered gates, but it enables us to investigate whether gate misalignment or varying L_{eff} can significantly improve the off-state leakage. Simulations show a clear trend of increasing the drive current with larger misalignment toward the drain (Fig.6). While drive current decreases with misalignment toward source, it improves the subthreshold slope.

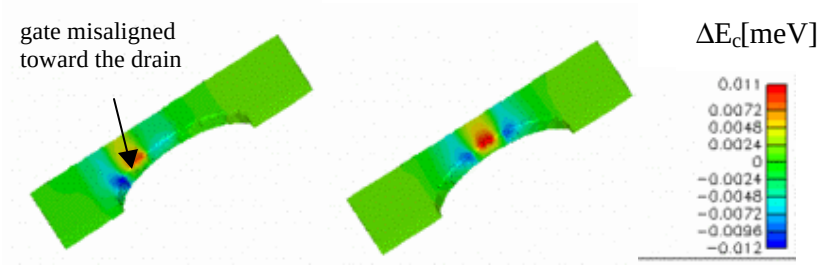

Fig.5: Change in the conduction band due to the stress in the devices with a misaligned gate (left) and with a centered gate (right). Only half width of the device is shown.

From our simulation results we extract effective mobility as $\mu_{eff}(V_{gs})=L^2*I_{ds}(V_{gs})/q/V_{ds}/N(V_{gs})$. The calculated effective mobility is much larger for misaligned cases than for the centered gates. The misalignment toward the source results in larger peak mobility, but it drops faster for larger vertical fields (Fig.7). Moving source/drain dopants away from the channel (i.e. increasing L_{eff}) improves I_{off}. This improvement is much more pronounced when misalignment is toward the drain. Fig. 8 shows I_{off} and I_{on} for L_{eff}, as defined above, between 14 and 20nm. The drive currents of centered gates are closer to the misaligned cases toward the source. But there is a large difference between centered cases and those misaligned toward the drain. This difference is larger for the small L_{eff}.

It is expected that 20nm devices will use thinner channels. We repeated simulations with 6nm thick channel. Fig. 9 shows transfer characteristics of a 20nm device with 6nm thick channel and 25nm gate misalignment, again showing larger drive current for transistors with larger width on the drain side. This time I_{off} is also acceptable for that case. The extracted effective mobility is shown in Fig. 10, showing a similar trend as for 10nm thick channels. Since surface roughness effects in thin silicon films are not taken into account, the mobility for thin channels is slightly larger than for thicker ones. Fig. 11 shows simulation results for different intrinsic stress in the gate. Tensile gate and misalignment toward drain give the highest drive current.

4 Conclusions

Our computer simulations show that in order to achieve manufacturable multi-gate narrow devices within expected lithographic limits underlaped devices will be required. Devices will have varying width and for our particular process devices with larger width on the drain side will benefit both in I_{off} and I_{on}. Process changes, especially intrinsic stress in the gate, can yield different results.

References

[1] S. Laux et al, *IEDM 2002*, p.715

[2] Z. Krivokapic et al, *SSDM 2003*, pp.760
[3] V. Moroz et al, *Materials Science in Sem. Proc.*, **6**, p.27-36,2003
[4] M. Ieong et al, in *Simulations of Semiconductor Processes and Devices*, editors K. De Meyer and S. Biesemans, pp. 129-132, Springer, Wien New York, 1998

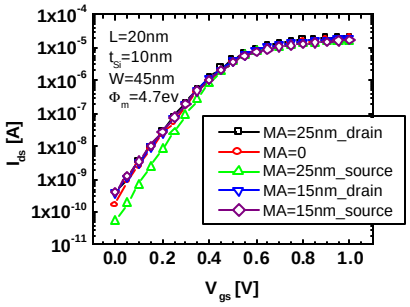

Fig.6: Simulated transfer characteristics for misaligned 45nm wide transistor (V_d=0.05V).

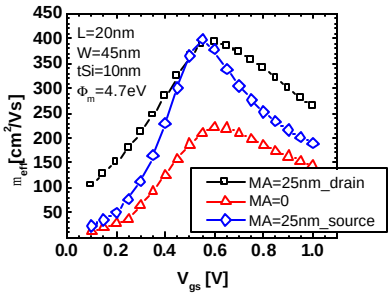

Fig.7: Effective mobility, extracted from simulated data for misaligned 45nm wide transistor (L_{eff}=20nm).

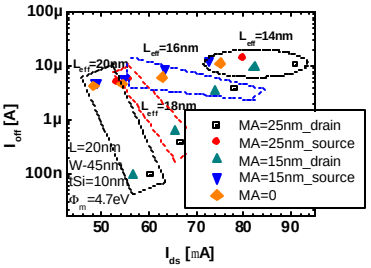

Fig.8: I_{on} and I_{off} for different misalignment and L_{eff}.

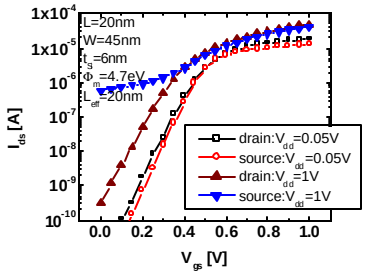

Fig.9: Transfer characteristics for narrow devices with channel thickness 6nm.

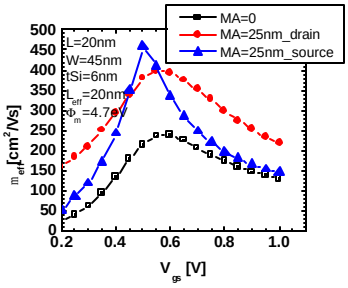

Fig.10: Effective mobility for thinner channel with intentional gate misalignment.

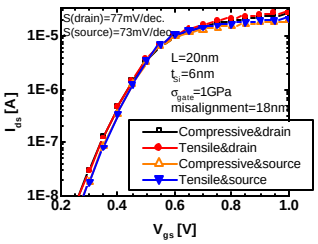

Fig. 11: Transfer characteristics for V_{ds}=50mV for devices misaligned by 18nm with compressive and tensile metal gates.