Examination of Spatial Frequency Dependence of Line Edge Roughness on MOS Device Characteristics

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Abstract

Full three-dimensional process and device simulations of short channel MOS transistors with gate edge roughness were performed. The amplitude and spatial wavelength of the edge roughness was varied systematically. Effects of correlated/anti-correlated right/left edge roughness were also investigated. Simulation results indicate that low spatial frequency anti-correlated edge roughness causes the worst degradation in device performance whereas low frequency correlated edge roughness causes the least device degradation. High spatial frequency edge roughness causes moderate device degradation, and the effect is independent of whether the gate edge roughness is correlated.

1 Background

The effect of line edge roughness (LER) has been studied extensively [1-6]. In [1], the effects of LER in both the front end of line as well as the back end of line have been presented. References [2-3] indicate that the effect of LER on devices is relatively small, although [2] claims that low spatial frequency LER is worse from a device point of view than high frequency LER. Croon *et al.* [6] show similar results but argues that LER will become more important as device gate lengths approach the 32nm regime. In light of this, a simple analysis method proposed in [7] showed that LER should affect devices adversely.

Although the analysis method proposed in [7] is quite fast and is believed to be a reasonable method to estimate the effects of LER, there are two salient LER features that can not be captured: 1) Spatial frequency dependence of LER on device characteristics, and 2) discerning the effect of edge roughness when the poly gate edges are perfectly correlated. Both of these effects are inherently 3-dimensional in nature. In this work, we perform a systematic analysis of the effects of edge roughness on device characteristics. We define devices with correlated and anti-correlated edge roughness as well as vary the spatial frequency of the LER.

2 Device Structure

The basic 3D structure is shown in Figure 1. We assume a bulk N-type MOSFET, with a uniformly doped substrate for simplicity. The concentration is adjusted so that the off current for a 35nm gate length device is 100nA/μm. A gate oxide thickness of

1.0nm is deposited followed by deposition of 0.1μm thick polysilicon pre-doped with n-type dopant to a level of 10^{20} cm^{-3}. A mask is defined and the gate is etched such that the poly gate has a rectangular bulge which is exactly half the total width of the device, and has amplitude, A, ranging from 0nm to 5nm. The device width is half the wavelength of the edge roughness. The quarter wavelength, L, varies from 2.5nm to 10nm. A 5keV, $1.5x10^{15}cm^{-2}$, 0 degree tilt As implant is performed, followed by a 1000C, 1s anneal. An amorphous target was assumed for the implant, and a simple Fermi model was assumed during the diffusion. Commercial software (Taurus process) was used in the process simulation. Default values were used for all parameters.

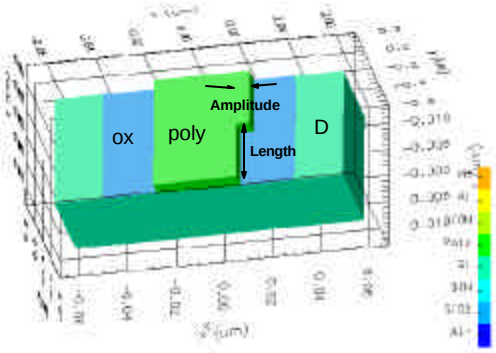

Figure 1. General structure that was studied. Edge roughness is defined by an Amplitude (A) and Length (L) . L is the quarter wavelength of the edge roughness.

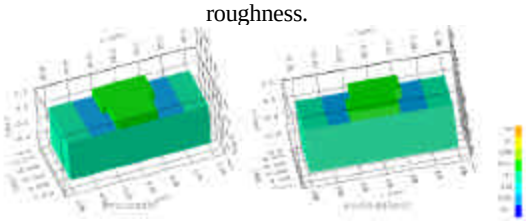

Figure 2. Devices with perfectly anticorrelated edge roughness (left structure) and perfectly correlated (right structure) edge roughness.

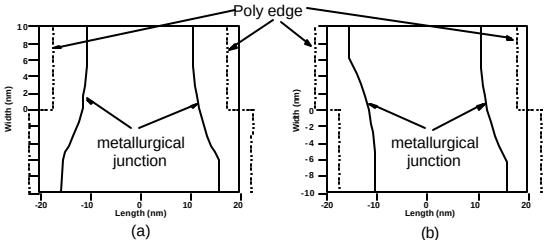

Figure 3. Metallurgical junction at the gate oxide/silicon interface. Quarter wavelength, L=10nm, and amplitude, A = 5nm. A) shows the junction edges for anticorrelated edge roughness. B) shows the junction edges for correlated edge roughness.

Figure 2 shows devices with correlated and anti-correlated edge roughness. The metallurgical junctions at the gate SiO_2/Si interface for large amplitude, long wavelength LER are shown in Figure 3. The metallurgical gate length for the correlated lines is smaller in the center of the device than at the edges. As the spatial frequency become higher, we would expect to see that the As implant at the edge of the gate to become more "smeared out".

To quantify if and when this occurs, we determine the separation between metallurgical junction locations as shown in Figure 4. For high frequency LER as shown in (a) and (b) of Figure 4, we see that the difference in metallurgical junction edges is relatively invariant with amplitude of the edge roughness. For low frequency LER, as shown in Figure 4(c), we see that the junction edge tracks with amplitude.

From the contour plot in Figure 5, we find that when the wavelength of the LER is greater than ~24nm, the junction edges track the amplitude of the LER. For wavelengths less than ~16nm, the metallurgical junction does indeed get "smeared out". For low amplitudes or low frequency LER, the implant and diffusion is mostly into the channel, for high frequency, large amplitude LER, a significant amount of implanted species scatters and diffuses into the width direction of the device. So, not only does the difference in junction edges reach a saturation value, but the average location of the junction is affected. For low amplitude, high frequency LER shown in Figure 4(a), the average junction location is at ~11.3nm, in Figure 4(b), the average junction location is at ~11.8nm, the difference between 4(a) and 4(b) being the amplitude of the LER.

3. Device Simulations

Since a typical 3σ value of edge roughness is on the order of ~8nm, and since [6] suggests that LER will become more significant at a gate length of ~32nm, we pick a gate length of 35nm as our target minimum. We assume that Vd=1V and our maximum off current will be ~100 nA/μm. Using a standard mobility model [8] in the Fielday device simulator [9], we simulate

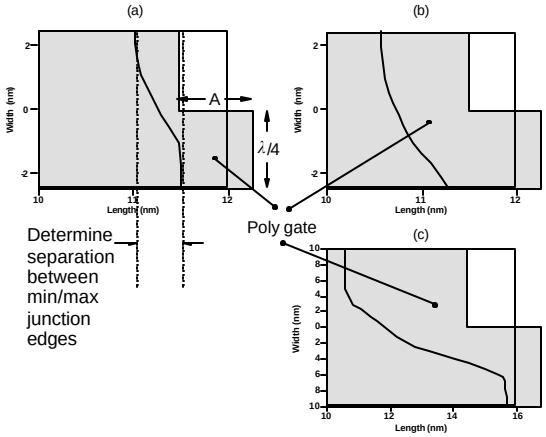

Figure 4. Analysis of the metallurgical junction edges. These 3 contour plots show how the junction edges vary for (a) high frequency, small amplitude (λ/4=2.5nm, A=1nm), (b) high frequency, large amplitude (λ/4=2.5nm, A=5nm) and (c) low frequency, large amplitude (λ/4=10nm, A=5nm) edge roughness.

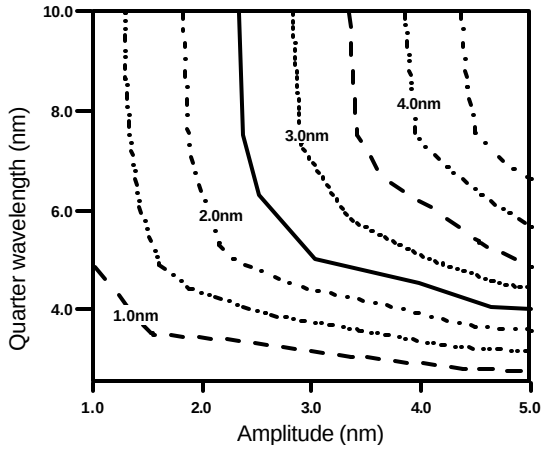

Figure 5. Contour plot of the difference in location of the junction edges as diagrammed in Figure 4. For low frequency edge roughness (quarter wavelength >~ 6nm), the difference in extrema of the junction edges tracks well with the amplitude of the edge roughness. For high frequency edge roughness, the difference in junction edge location is independent of the amplitude of the edge roughness.

typical device characteristics for a 35nm device with edge roughness. Simulations show that the on currents are independent of the spatial frequency until the LER amplitude becomes quite large. This is true for both correlated and anti-correlated edge roughness.

We extract an equivalent gate length by simulating the inversion capacitance and scaling it by Cinv for the 35nm device without LER. When we do this, we find that the off current behaves similarly to the on current. As the edge roughness amplitude increases, the effect of the increased overlap capacitance causes the gate length extraction to become skewed to longer gate lengths. Figure 6 shows an analysis of the Ioff/Ion characteristics. For perfectly correlated long wavelength LER, the Ioff/Ion characteristics are similar to a device with no LER. High frequency LER, whether correlated or anti-correlated shows worse Ioff/Ion characteristics, but long wavelength anti-correlated LER shows that off current is most adversely affected. Furthermore, we show significant deviations from the 2D slice analysis, indicating that the simplified analysis in [7] is not as valid as originally shown.

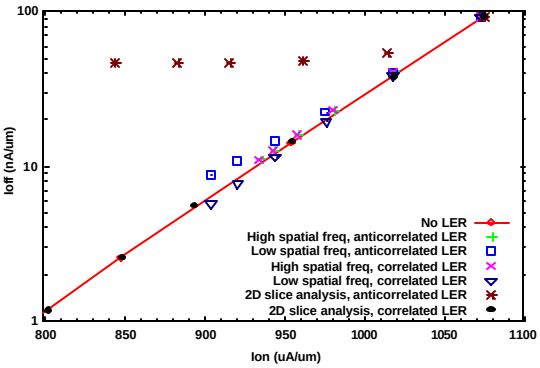

Figure 6. Ion/Ioff variation for devices with no edge roughness compared to devices with edge roughness. Devices with high frequency edge roughness show higher off current at longer equivalent gate lengths.

4. Summary

3D process and device simulations were performed indicating that the effect of edge roughness depends on the spatial frequency of the variations and whether the edge roughness is correlated or anticorrelated. Devices with correlated edge roughness behave as though there is no gate edge roughness. High frequency edge roughness shows fewer deleterious device effects than low frequency edge roughness.

References

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