Hole Mobility Enhancement Modeling and Scaling Study for High Performance Strained Ge Buried Channel PMOSFETs

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Abstract

In this work, we simulated the long channel Ge-buried channel PMOSFETs by using drift-diffusion equation and calibrated the commonly used silicon mobility model to take buried channel hole mobility enhancement into account. 2D simulations were performed to study the channel design space for strained Ge buried channel PMOSFETs and two different buried channel structures were proposed to control short channel effect (SCE) down to 30nm channel length.

1 Introduction

In recent studies, dramatic hole mobility enhancement has been demonstrated in strained Ge (s-Ge) buried channel (BC) MOSFETs with relative thick Si capping layers [1,2,3]. Though Si capping layers eliminate the poor interface between the gate oxide and the pure Ge channel, they do not allow scaling to short channel lengths. In this work, a calibrated silicon mobility model was utilized to account for the buried channel hole mobility enhancement by comparing drift-diffusion simulations of long-channel s-Ge BC PMOSFETs to experimental ring-shaped MOSFETs. Using this calibration, we have performed 2D simulations to study the scalability of deep sub-100 nm s-Ge BC PMOSFETs with a Si cap thickness of 2 nm.

2 Mobility Calibration

Ring shaped, long channel MOSFETs were fabricated using a one-mask process as shown in Fig. 1 and the linear regime Id-Vgs characteristics were measured [5].

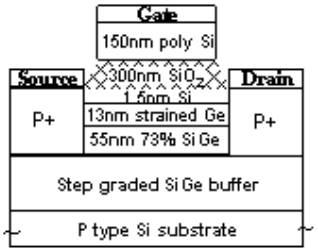

Fig. (1) Schematic cross section of the Strained-Ge buried channel PMOSFETs.

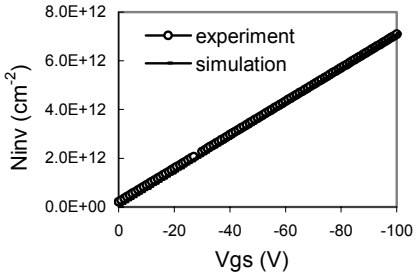

Fig. (2) Measured and simulated 2D inversion carrier density vs. gate voltage at Vds=50mV.

Drift-diffusions simulations were performed on the structure shown in Fig. 1. using the FIELDAY device simulator [4]. The buried s-Ge layer and relaxed SiGe buffer were taken into account by using appropriate band offsets in the defined device. First, the valence band-gap offset dEv of the Ge channel was adjusted to 0.465eV to match the experimental inversion charge density (see Fig. 2). Next, we adjusted scattering parameters in the Mujtaba mobility model [6] to fit the Ids-Vgs characteristics, shown in Fig. 3. Because the

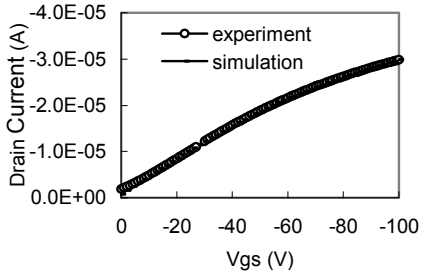

Fig. (3) Measured and simulated linear Ids-Vgs characteristics for the long channel (Lg=100um) BC PMOSFET at Vds=50mV.

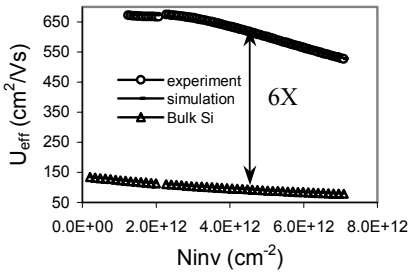

Fig. (4) Measured and simulated effective hole mobility vs. inversion charge density. Effective hole mobility of strained Ge BC PMOSFETs is more than 6X enhanced over the Si bulk universal hole mobility.

device we fabricated is lightly doped (1e15cm-3), carrier-carrier scattering does not affect mobility. We adjusted the surface roughness component of the mobility by increasing it by a factor of 6X, which suggests that surface roughness scattering is greatly reduced in the buried channel. Although we assumed that the BC PMOSFET has the same mobility – transverse field relationship as conventional silicon device, the excellent fit of the Ids-Vgs data in Fig. 3 validates our assumption. In the low to moderate transverse field region where the phonon scattering dominates, the Mujtaba model uses an expression of the form $\min\left(B/E_t + C\cdot(N_A+N_D)^{\gamma}/(T\cdot E_t^{1/3}), U_L(300/T)^{\mu_L}\right)$. Our analysis showed that the UL term is chosen in the low field region and the B+C term determines the phonon limited mobility when the transverse field becomes larger. We adjusted UL to 1.41xUL^{Si} and C to 9.68 x C^{Si} to match I-V experimental data as shown in Fig. 3 The mobility enhancement observed in s-Ge BC PMOSFETs, as shown in Fig. 4, is found due to the significantly reduced phonon and surface roughness scattering. The reduced surface roughness scattering is mainly coming from buried channel operation, while the reduced phonon scattering is due to the compressively strained Ge channel.

3 Scaling of Strained Ge Buried Channel Devices

From our previous studies [5], 1D electro-static simulations show that in order to keep the carriers with high mobility in the buried channel, a low channel doping concentration is desirable. On the other hand, low substrate and channel doping make it difficult to control the SCE in sub-100nm strained Ge buried channel devices. In this work, two structures were proposed to control the SCE: (1) a bulk device with a retrograde doping profile; and (2) a buried Ge channel on insulator (BCGOI) device with lightly doped channel as shown in Fig. 5. For the bulk device, Fig. 6 shows that a retrograde doping profile helps to confine carriers in the BC (e.g. for a 2nm Si-cap layer BC device, the carrier density in the BC increases by 5X using a retrograde doping compared to that of a

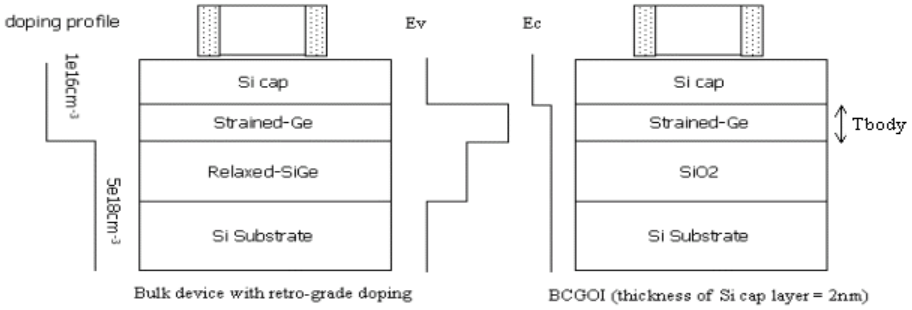

Fig. (5) Energy band offset, layer structures and retrograde doping profile of strained Ge BC PMOSFETs used in device simulation (left: bulk device with retrograde doping, right: BCGOI).

constant doping profile). A comparison of the subthreshold behavior of BC and Si surface-channel (SC) devices with retrograde doping profiles is shown in Figs. 7 and 8. The

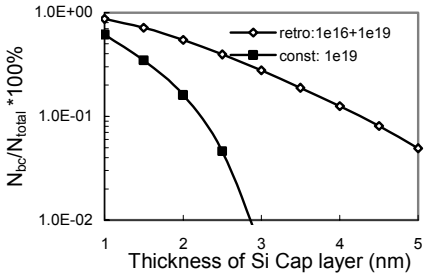

Fig. (6) The percentage of carriers in the buried channel over the total carriers at Q_{inv}=1e13cm^{-2} as a function of Si cap thickness for constant doping and retrograde doping profiles.

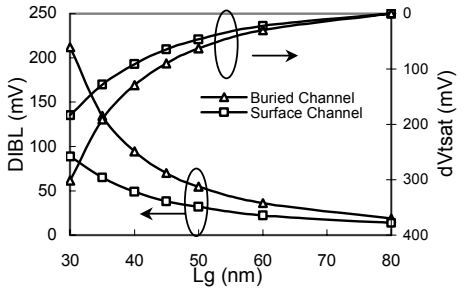

Fig. (7) Vtsat roll-off characteristics and DIBL of s-Ge BC PMOSFETs as compared to the Si surface channel device with a retrograde doping profile of 1e16cm^{-3}+5e18cm^{-3} as shown in Fig.5.

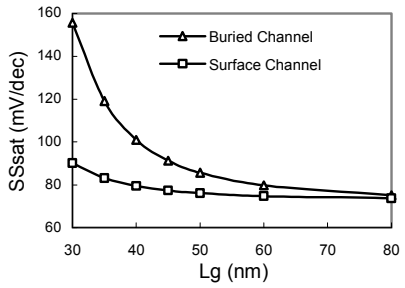

Fig. (8) Subthreshold swing vs. gate length of s-Ge BC PMOSFETs as compared to the Si surface channel device with a retrograde doping profile of 1e16cm^{-3}+5e18cm^{-3}.

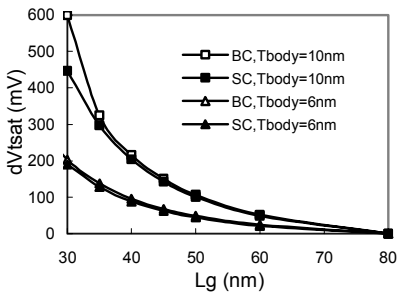

Fig. (9) Vtsat roll-off characteristics of s-Ge BC PMOSFETs with different channel thickness as compared to the SOI surface channel (SC) devices.

figures show that when the channel length is scaled down to 40nm, even though the BC device shows worse DIBL and Vt roll-off than those of the surface channel device, the SCE is still under control. However, the benefits of the retrograde profile are minimal for

channel-lengths below ~40 nm. Further improvement in the short-channel characteristics can be achieved using the second BCGOI structure, by shrinking the body thickness. The channel doping in BCGOI is 1e16cm-3, and more than 90% of the carriers are confined in the BC over the operating voltage range. Figs 9-11 show that BCGOI devices exhibit similar short channel characteristics to those of conventional surface channel SOI devices.

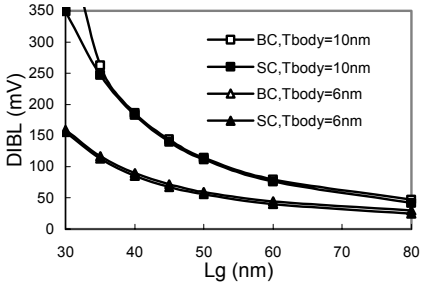

Fig. (10) DIBL of s-Ge BC PMOSFETs with different s-Ge layer thickness as compared to the SOI (SC) devices. Thinner s-Ge thickness gives better SCE control.

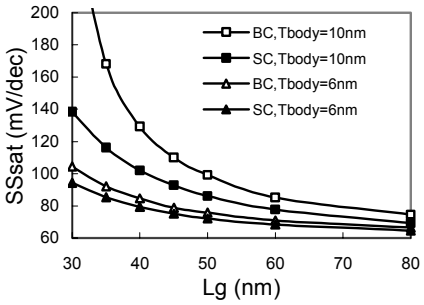

Fig. (11) Subthreshold swing vs. gate length of strained Ge BC PMOSFETs as compared to the SOI (SC) devices. A body thickness of 6nm BCGOI devices can be scaled down to 30 nm.

4 Summary

In conclusion, we have accurately calibrated the hole mobility for Ge buried channel PMOSFETs for use in device simulations to predict BC device performance. The calibration shows that greater than 6X hole mobility enhancement over the Si universal hole mobility can be achieved due to greatly reduced phonon and surface roughness scattering. In addition, 2D simulations were performed to study the scalability of deep sub-100 nm strained Ge buried channel PMOSFETs with a 2nm Si cap layer. Two device structures are proposed to control SCE in BC devices down to 30nm channel length.

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