Comparison of Nanoscale Metal-Oxide-Semiconductor Field Effect Transistors

Yiming Li[1,2,*], Jam-Wem Lee[1], Hong-Mu Chou[3]

[1]Dept. of Computational Nanoelectronics, Nat'l Nano Device Lab.
[2]Microelectronics & Information Systems Research Center, Nat'l Chiao Tung Univ.
[3]Dept. of Electrophysics, National Chiao Tung Univ.
[*]P.O. BOX 25-178, Hsinchu 300, TAIWAN; E-mail: ymli@mail.nctu.edu.tw

Abstract

In this paper, electrical characteristics of nanoscale single-, double-, and all-around-gate silicon-0n-insulator (SOI) devices are computational investigated by using a quantum mechanical simulation. Considering several important properties, such as on/off current ratio, drain induced channel barrier height lowering, threshold voltage roll off, and subthreshold swing, geometry aspect ratio is systematically calculated and characterized among structures. To obtain good operation characteristics, the ratio of channel length and silicon film thickness should be optimized with respect to device structures.

1 Introduction

Double- and all-around-gates silicon-on-insulator (DG and AG SOI) devices have recently been of great interest; in particular for sub-10 nm device applications [1-14]. Compared with the single-gate (SG) SOI, these structures suppress short channel effects (SCEs), and have high transconductance and ideal subthreshold swing. They have a superior ability in channel control, so the drain induced channel barrier height lowing (DIBL), threshold voltage (V_{th}) roll off, and off state leakage is greatly suppressed [1-7]. The structure can be subject to further optimization to sustain more structural benefit. In this paper, we compare electrical characteristics for sub-10 nm SG, DG, and AG SOI metal-oxide-semiconductor field effect transistors (MOSFETs) using a quantum mechanical simulation. Based on our own nanodevice simulator, devices with different channel lengths (L_g) and silicon film thicknesses (T_{si}) are simulated and analyzed to have an optimal configuration [8-14]. We conclude that the silicon film thickness pays an important factor in eliminating SCE. To suppress SCE in sub-10 nm SOI MOSFETs, the thickness of the silicon film must be scaled down simultaneously. Among structures, the studied cylindrical all-around-gate FET shows promising characteristics for nanodevice applications. Different channel length to silicon film thickness ratios are numerically observed with respect to different structures.

2 Computational Model

As shown in Fig. 1, three device structures: SG, DG, and AG SOI devices are explored numerically. Because these devices are in the nanoscale regime, it has become necessary to include quantum mechanical (QM) effects when modeling device behavior; in particular, for such sub-100 nm devices. There have been several approaches

to the modeling of QM effects [8-14]. Among them, full QM methodology physically plays an accurate way to simulate nanodevices. However, it costs expensive in TCAD simulation of multi-dimensional nanodevices. A calibrated density gradient equation together with hydrodynamic model is used in the simulation of nanoscale FETs. It is computationally effective for combining QM effects in 2D/3D device simulation. Our computational experiences in sub-10 nm FETs indicate this approach is behavior qualitatively consistent with source/drain tunneling.

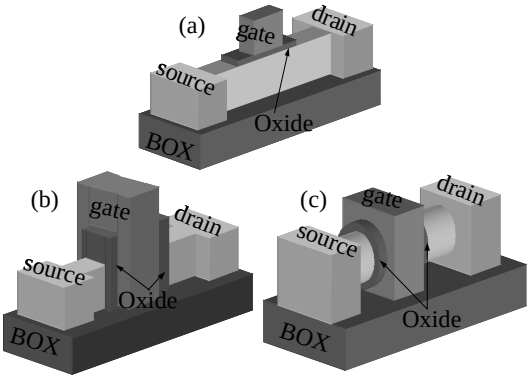

Figure 1: Schematic diagrams for (a) SG, (b) DG, and (c) AG SOI devices.

3 Result and Discussion

The source/drain of studied (S/D) n-type SOI FETs is $10^{19}\ cm^{-3}$, the S/D contact is $10^{20}\ cm^{-3}$, and the channel doping is $10^{15}\ cm^{-3}$ uniformly. The oxide thickness is fixed at 1 nm for all structures [1-14]. Fig. 2 shows the $I_D - V_G$ characteristics of devices fabricated on 10 nm thicken silicon film. It is found that the shorter channel length leads to the worse SCE. That is, V_{th} is continuously decreasing with the increment of drain bias. Due to the fully depleted channel effect, the thin body devices' V_{th} becomes relatively low, and is hard to adjust by changing the channel doping. Consequently, developing the new mid-band material for gate formation becomes an important course. After comparison among three structures, we find that the AG FET exhibits a better SCE in 5 nm lengthen gate; however, few benefits could be obtained when $L_g > 10$ nm. The on/off current ratio, subthreshold swing, threshold voltage roll-off and the DIBL effect of the three devices are summarized in Tables 1 and 2, respectively. The SG SOI devices show unacceptable characteristics for all cases. It implies that SG structures may not continuously suit for sub-10 nm generation. The cylindrical-shaped all-around-gate structure demonstrates much better characteristics for all evaluated parameters. However, if we take the complexity of fabrication processes into consideration, this structure will be more suitable for the ratio of $L_g/T_{si} < 1$. Shown in tables, "–" means that it is out of definition.

Structures		On/Off ratio			SS (V/decay)		
		SG	DG	AG	SG	DG	AG
T_{si}= 10 nm	L_g=5 nm	1.31×10^{3}	1.17×10^{6}	3.84×10^{7}	0.4225	0.086	0.072
	L_g=10 nm	3.75×10^{4}	4.76×10^{7}	1.14×10^{9}	0.1277	0.0685	0.0675
	L_g=20 nm	3.73×10^{6}	1.07×10^{9}	1.11×10^{10}	0.0875	0.0679	0.0671
T_{si}= 20 nm	L_g=5 nm	24.24	2.95×10^{3}	1.17×10^{5}	–	0.1909	0.0879
	L_g=10 nm	115	1.41×10^{5}	1.78×10^{7}	0.4371	0.1117	0.0719
	L_g=20 nm	3.64×10^{3}	1.99×10^{7}	6.04×10^{8}	0.1747	0.0815	0.0693

Table 1: The on/off current ratio and subthreshold swing (SS) of the simulated FETs.

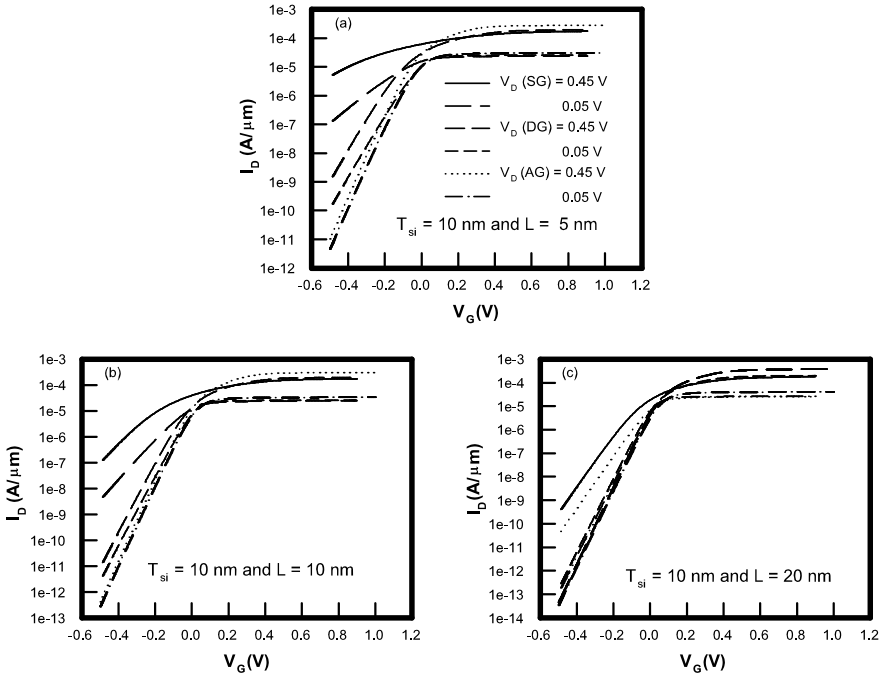

Figure 2: The simulated $I_D - V_G$ characteristics for SG (solid and long dash lines), DG (dash and short dash lines), and AG (dot and dash-dot lines) FETs.

4 Conclusions

We explored characteristics of SG, DG, and AG SOI FETs with our quantum mechanical-based device simulator. It has been found that T_{si} should be scaled down with L_g simultaneously, and a thinner T_{si} will greatly suppress the short channel effect. Simulation suggests that $L_g/T_{si} > 3$, 1, and 1/2 for SG, DG, and AG SOI devices, respectively, will provide acceptable physical characteristics. However, if we additionally consider the practical device characteristics and process complexity, the ratio can vary from 1 to

Structures		V_{th} (V)			DIBL (V)		
		SG	DG	AG	SG	DG	AG
T_{si}= 10 nm	L_g=5 nm	–	-0.2784	-0.0181	–	0.0727	0.045
	L_g=10 nm	-0.4015	-0.1926	-0.0176	–	0.0674	0.0224
	L_g=20 nm	-0.2331	-0.1725	-0.0113	0.0112	0.027	0.015
T_{si}= 20 nm	L_g=5 nm	–	-0.2136	-0.1951	–	0.2635	0.093
	L_g=10 nm	–	-0.1613	-0.1051	–	0.1415	0.0508
	L_g=20 nm	-0.2852	-0.0994	-0.0513	–	0.0514	0.0278

Table 2: The calculated V_{th} and DIBL of the simulated FETs.

3 for the DG SOI. For the cylindrical AG FET, it varies from 1/2 to 1.

5 Acknowledgement

This work is supported in part by TAIWAN NSC grant: NSC-92-2112-M-429-001 and the grant: 92-EC-17-A-07-S1-0011 from Ministry of Economic Affairs, Taiwan.

References

[1] H. Wakabayashi et al., "Sub-10-nm planar-bulk-CMOS devices using lateral junction control", Tech. Dig. IEDM, p. 20.7, 2003.

[2] M. Ogawa et al., "Quantum transport modeling in nano-scale devices", Proc. IEEE SISPAD, pp. 261-266, 2002.

[3] M. Ieong et al., "High performance double-gate device technology challenges and opportunities", Proc. IEEE ISQED, pp. 492-495, 2002.

[4] X. Huang et al., "Sub 50-nm FinFET: PMOS ", Tech. Dig. IEDM, pp. 67-70, 1999.

[5] Y. Li et al., "Comparison of quantum correction models for ultratin oxide single- and double-gate MOS structures under the inversion conditions", Proc. IEEE-Nano, pp. 36-39, 2003.

[6] J. H. Rhew et al., "A numerical study of ballistic transport in a nanoscale MOSFET", Solid-State Elec. vol. 46, pp. 1899-1906, 2002.

[7] T. J. Walls et al., "MOSFETs below 10nm: quantum theory", Physica E vol. 19, pp. 23-27, 2003.

[8] A. Asenov et al., "Quantum corrections in the simulation of decanano MOSFETs", Solid-State Elec. vol . 47, pp. 1141-1145, 2003.

[9] V.A. Sverdlov et al., "Nanoscale silicon MOSFETs: A theoretical study", IEEE Trans. ED vol. 50, 1926-1933, 2003.

[10] A. Asenov et al., "The Use of Quantum Potentials for Confinement and Tunnelling in Semiconductor Devices", J. Comput. Elec. vol. 1, pp. 503-513, 2002.

[11] Y. Li et al., "Numerical Simulation of Quantum Effects in High-k Gate Dielectrics MOS Structures using Quantum Mechanical Models", Comput. Phys. Commun., vol. 147, pp. 214-217, 2002.

[12] Y. Li et al., "A Practical Implementation of Parallel Dynamic Load Balancing for Adaptive Computing in VLSI Device Simulation", Eng. Comput., vol. 18, pp. 124-137, 2002.

[13] R. Venugopal et al., "Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches", J. Appl. Phys., vol. 92, 3730-3739, 2002.

[14] Y. Naveh et al., "Modeling of 10-nm-scale ballistic MOSFET's", IEEE ED Lett., vol. 21, pp. 242-244, 2000.