CMOS Scaling Analysis based on ITRS Roadmap by Three-dimensional Mixed-mode Device Simulation

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Abstract

In this paper, the circuit performances such as circuit delay, RF characteristics and SRAM static noise margin are presented. These analyses are performed by three-dimensional device simulation using Mixed-mode option. The benefit of circuit delay in scaling will be maintained by introducing new structure (SOI, multi-gate), material (silicide, metal gate) and strain effect. However, concerning with SRAM SNM, it becomes already difficult to operate even in 65nm node.

1 Introduction

The device whose gate length is below 50nm begins to appear in a market, and the operation of 5nm gate length device was presented in IEDM 2003 [1]. However, it will be very difficult to maintain the performance enhancement by scaling as it has been in the past. Although transistor level simulations of single gate (SG), double gate (DG) SOI devices, non-planar devices such as FinFET [2] and TriGate devices, high-k dielectric film and strained-Si channel device [3] have been already done, the circuit performance evaluations for these devices are very few and are only limited in two-dimensional. The reasons are that compact modeling has not been fully developed and calculation cost of three-dimensional simulation is very expensive. And in recent years, because MOSFET is adapted in high frequency circuits in place of bipolar transistor, it becomes very important to analyze radio-frequency (RF) characteristics for analog applications.

In this paper, we evaluate the circuit performance such as inverter, RF characteristics and SRAM static noise margin (SNM) by three-dimensional Mixed-mode device simulation. Finally, we will show the perspective in the future.

2 Simulation Method

We evaluated three technology nodes: 65nm, 45nm, and 22nm node. Device structure parameters were decided according to ITRS roadmap [4]. Table 1 shows the calculated parameters. We used the ISE device simulator DESSIS and Mixed-mode options were used in the circuit analysis. The transport model was Hydro-Dynamic model.

Table 1 : Parameters of calculated devices.

Year	2007	2010	2016
Technology Node (nm)	65	45	22
Gate Length (nm)	25	18	9
Oxide Thickness (nm)	1.1	0.8	0.5
Supply Voltage (V)	0.7	0.6	0.4
Off-state Current (μA/μm)	1	3	10

Calculated structures were SG, DG and TriGate devices. SG and DG devices were simulated in 2D and TriGate device was in 3D simulation. The flowchart of the evaluation procedure is shown in Fig. 1. First, to meet off-state leakage specifications, gate work function was adjusted by device simulation. Second, by Mixed-mode simulation, we calculated the delay characteristics of fan-out four (FO4) inverter. Then we calculated maximum frequency of oscillation (f_{max}) in each NMOS device and analyzed the RF characteristics. As for strained-Si mobility model, we used the built-in model in DESSIS which is based on biaxial tensile strain mobility model calculated by Monte Carlo simulation [5]. Finally, we calculated SRAM SNM.

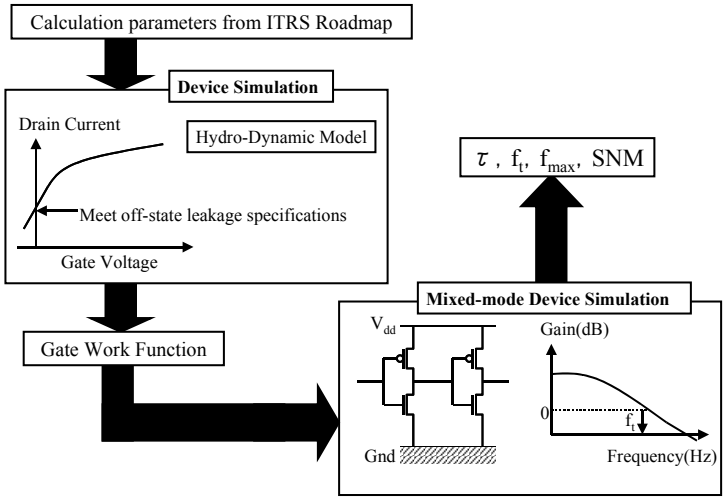

Fig. 1 : The flowchart of the evaluation procedure.

3 Results and Discussion

In Fig. 2, the FO4 inverter circuit delay characteristics are shown. In this simulation, wire capacitance and parasitic resistance are not included. In SG device, delay improvement will be expected only below 2nm body thickness. On the contrary, in DG, delay characteristic will be enhanced with 5nm body thickness. This difference is

mainly due to the controllability of short channel effect (SCE). This result shows suppression of SCE will be more and more crucial in future scaling. In TriGate, enhancement ratio due to scaling is the same as DG device, but the speed is only improved by about 20 %. This is because of corner edge electric-field enhancement. In the case of strained-Si channel device, which has 10% Ge content SiGe buffer layer, delay improvement will be expected to be about 20%. Compared with the delay characteristics demand from the ITRS roadmap, it was found that, in 65nm node, SG SOI structure and, in 45nm node, SG SOI + strained-Si channel device or TriGate device and, in 22nm node, TriGate + strained-Si channel device will meet the ITRS requirement. This result also meets the new material and structure description in ITRS 2003.

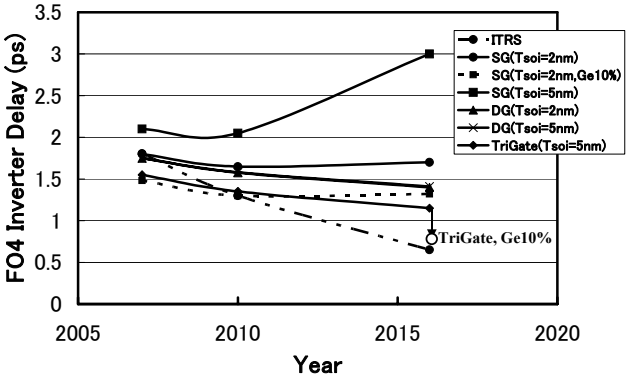

Fig. 2 : Circuit delay characteristics of FO4 inverter.

Fig.3 demonstrates the RF characteristics. Compared with roadmap, SG will be difficult to satisfy a demand in 45nm node, and DG and TriGate will also in 22nm node for poly silicon gate. As gate length is scaled down, gate resistance will increase dramatically. So the gate resistance effect on f_{max} becomes increasingly problematic. By using silicide and metal gate with vely low gate resistance, we can expect further scaling.

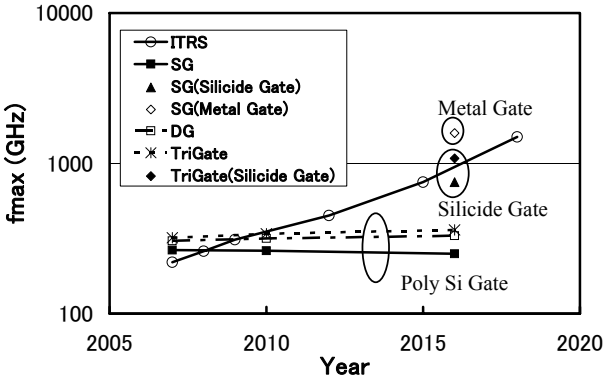

Fig. 3 : The maximum frequency of oscillation.

Finally, Fig.4 shows SRAM SNM. As a target value, $0.15*V_{dd}$ value is drawn in this figure. In 65nm node, even TriGate is difficult to meet the circuit demand. Although device performance requirement in circuit delay will be maintained, noise margin might be the limitation factor for further scaling. In order to keep scaling further more, SRAM operation must be carefully designed

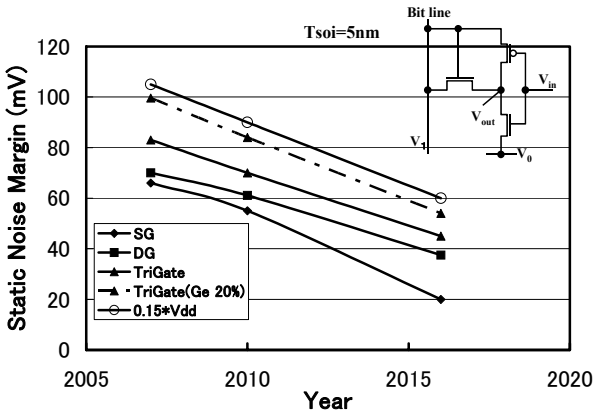

Fig. 4 : SRAM static noise margin

4 Conclusion

By performing the three-dimensional device simulation using Mixed-mode operation, circuit delay, RF characteristics and SRAM SNM were analyzed. The benefit of circuit delay and RF characteristics in scaling will be maintained by introducing new structure, material and strain effect. However, concerning with SRAM SNM, it becomes already difficult to operate even in 65nm node. This implies that improvement of SRAM characteristics may be one of the most critical issues for future scaling.

References

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