# Adaptive Surface Triangulations for 3D Process Simulation

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**Abstract**

We present an enhanced smoothing algorithm in order to minimize the number of nodes in a surface triangulation while at the same time the wafer topography is maintained, and changes of geometry are limited to user-defined tolerances. Refined criteria for the protection of nodes and edges which have not to be removed because of topological reasons have been worked out. An algorithm has been implemented for the extraction of local smoothing tolerance. The use of local and material-dependent smoothing tolerance is mandatory for the optimization of surface triangulations. Our topologically correct smoothing algorithms with user-controlled tolerances provides large opportunities for increased efficiency of 3D simulation of various process steps. Some examples for this application are given.

## 1 Introduction

The simulation of advanced device architectures such as FinFET transistors increasingly needs to be done in three dimensions (3D): Here, 3D effects are not only quantitative corrections as e.g. for the dependence of threshold voltage on width in POCKET transistors [1], but they even qualitatively affect device behavior since there is no more a 2D cut plane existent which may be used to describe the device in an appropriate approximation [2]. However, especially 3D process simulation is still hampered by limitations in topography simulation, surface and volume meshing, in spite of the large progress during the last years. This paper addresses the adaptation of surface triangulations and its benefits to volume meshing and especially to the 3D simulation of process steps. Emphasis is put on coarsening which is in meshing mostly more difficult than refinement.

## 2 Topography Simulation Using Triangulated Surfaces

We have successfully used triangulated surfaces for the 3D simulation of deposition steps [3]. In that implementation, adaptive mesh refinement was necessary and done at convex corners. The removal of triangles with very small height to avoid their collapsing was the only coarsening step done. This means that the number of triangles usually increases during simulation, which may cause problems with other process steps or volume meshing as mentioned below. Furthermore, some of the physical models used in deposition simulation need the space angles covered by each other triangle w.r.t. the point in question, including shadowing calculations. Looking at this

in some detail the computation time for the shadowing calculation scales approximately with the number of surface triangles - so coarsening would is highly beneficial.

## 3 Topologically Correct Smoothing

The basic principle of a smoothing algorithm which removes points from a surface triangulation as far as this does not change the device geometry more than a predefined tolerance was presented earlier [4]. This smoothing can only be efficient if triangle points which are part of mask edges are correctly treated: Those are points which are adjacent to at least three layers – so called triple points. Most of these are linked together to so-called triple lines, e.g. that line where the yellow spacer in Fig. 1 meets the blue oxide (and the white air). In [4] topological criteria for the removal of such triple points are discussed which make sure that such smoothing does not change the topology of the device, e.g. by opening or closing windows or holes in a layer. Points where removal is not forbidden due to these topological criteria may be removed if geometrical criteria are met: The distance of the smoothed triple line from the original one must be within a given tolerance to make sure that e.g. the position of a tilted mask edge or the edge of a thin layer are not changed too much, because otherwise the process results may be critically affected. In this paper we discuss the geometrical criteria used and implemented, which are among others based on the local thickness of layers (distance to other interfaces) and the material of the neighboring layers: Tolerances must be completely different e.g. for a nanometer gate oxide and for a thick field oxide. In result the algorithm enables the coarsening of surface triangulations, maintaining the device topology (=connectivity of layers, existence or non-existence of holes, etc.) and keeping the changes of the device geometry within local tolerances which depend on the neighboring materials, the distance to other interfaces, and user-defined requirements (e.g. relative and absolute error). However, this adaptation does not consider triangle quality criteria such as the Delaunay property.

## 4 Application to Enhance Efficiency of 3D Process Simulation

The capability not only to refine but also to unrefine surface triangulations without changing topology and with controlled error in geometry has a wide set of applications in 3D process simulation:

First and most obvious, a surface triangulation with a smaller number of nodes also allows for a 3D volume mesh with a smaller number of nodes, if one assumes that each node and edge of the surface triangulation must also be part of the volume mesh. If that latter requirement would not be met, because the volume mesher may neglect surface nodes or flip surface edges, then an unpredictable change especially of device topology may occur. On the other hand side, it is much easier to control the insertion of additional nodes in a surface triangulation by the volume mesher, in order to achieve sufficient volume mesh quality.

Second, coarsening of surface triangulations increases the efficiency of triangle-based 3D topography simulation in several ways. The straight-forward application is to apply a coarsening step with appropriate tolerances before continuing deposition or etch simulation with the coarser triangulation. Even more interesting is to use a coars-

ened triangulation only for calculations required by the physical model in deposition and etching steps, e.g. when calculating visibility between surface patches and between surfaces patches and gas.
Third, coarsening of surface triangulations is also very valuable for the 3D simulation of ion implantation. We presented earlier a very efficient 3D program for the simulation of ion implantation using analytical models which employs an appropriate projection of all surface triangles onto a plane [5]. Within this plane the 2D convolution integrals which are part of the usual analytical models can be calculated very efficiently. This basically separates between processing of the surface and calculation of the convolution integral, which drastically enhances speed. Surface coarsening with a tolerance small compared to the range straggling of the implanted ions now hardly affects the resulting dopant contributions. Moreover, an error estimate can be easily given assuming Gaussian distributions for that estimate.

## 5 Example

Fig. 1 shows the 3D simulation of a typical 180 nm STI transistor using the extension of the software environment from ISE AG [6], developed in the MAGIC_FEAT project [7]: Left the structure resulting from 3D process simulation, right that after coarsening with appropriate local tolerances which are e.g. larger for the spacer (yellow) than for the oxide and silicon. Here, coarsening with 1 Å tolerances has reduced the number of surface and interface triangles from 30133 to 3548. Fig. 2 shows the result after 3D simulation of As implantation at 100 keV with a dose of $10^{15}$ $cm^{-2}$. In turn, the CPU time for 3D implantation simulation is decreased from 24 to 12 min on a typical PC. No change of the implanted dopant profiles is visible in the 3D distributions or along a horizontal line as shown in Fig. 2c. The maximum error along this cut is about 1.5%. The deviations between both simulations, shown in the vertical profile in Fig. 2d, result from the interpolation done to extract this 1D cut from the data on the unstructured tetrahedral mesh used in the simulation.

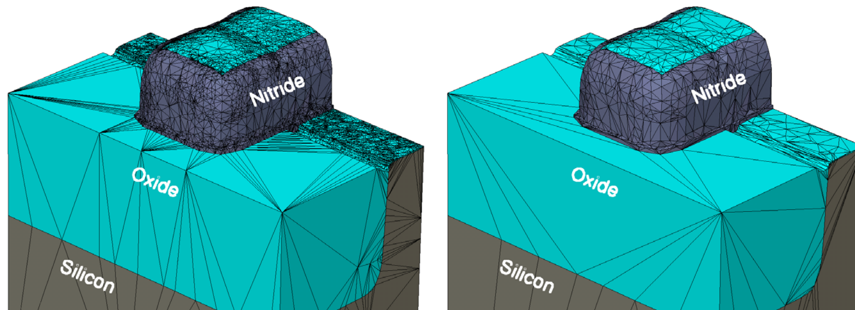


**Fig. 1:** 3D simulation of a 180 nm STI Transistor. Left: Surface triangulation after 3D process simulation; right: surface triangulation after coasening

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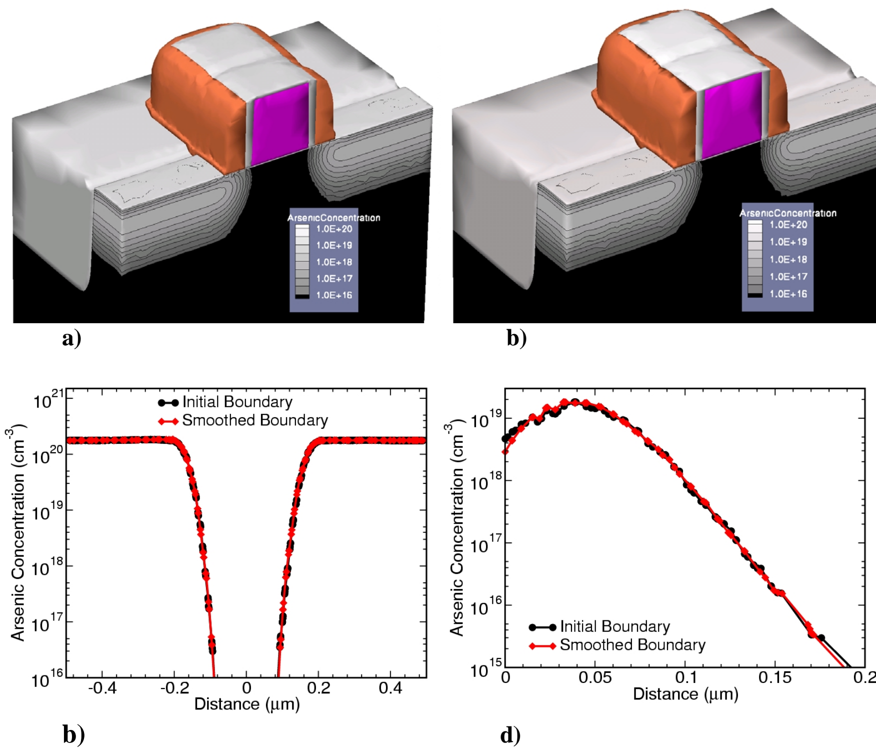


**Fig. 2:** Dopant distribution in STI transistor of Fig. 1 after implantation of As at 100 keV with a dose of $10^{15}$ $cm^{-2}$. Upper row: 3D distribution using the original (a) and the smoothened surface triangulation (b). Lower row: 1D profile along horizontal line from source to drain connecting maximum source and drain concentrations (40 nm below silicon surface) (c) and along vertical line through middle of spacer (d), both in the front plane of upper figures.

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