3D Simulation of Process Effects Limiting FinFET Performance and Scalability

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Abstract

Coupled three-dimensional process and device simulations have been applied to study effects limiting the performance of FinFETs, a novel CMOS transistors suggested to overcome the limitations of conventional CMOS for gate lengths at 50 nm and below.

1 Introduction

Further development of CMOS technologies as projected e.g. by the International Technology Roadmap for Semiconductors is more and more challenged by basic physical limits e.g. on oxide thickness, material properties, statistical fluctuations, and spread of process results (3σ variations). This paper presents enhancements of three-dimensional (3D) process simulation and results concerning some critical effects of fabrication steps and their tolerances on the FinFET transistor [1] which is a promising candidate for upcoming generations of CMOS devices.

2 Improvement and Application of 3D Process Simulation to FinFET Simulation

The FinFET utilizes SOI substrates. It is fabricated by patterning of a thin silicon film on top of a buried oxide to create a stripe of silicon which connects source and drain. The gate partly surrounds this silicon stripe, see Fig. 1. Different from wide planar CMOS transistors the FinFET transistor cannot reasonably be approximated by a 2D cross section along the gate axis. As shown below in Figs. 1 c) and d), e.g. the drain current is highly inhomogeneous within a cross section vertical to the channel. Among others, in [2] the inverse corner effect in FinFET transistors was presented. Therefore, for this device architectures 3D simulations are absolutely mandatory. This motivates the work presented.

The fabrication of FinFETs has been simulated with the 3D process simulation environment from the MAGIC_FEAT project [3] which is an extension of the software environment from ISE AG [4]. Here, the device geometry is described by triangulated surfaces, which are also used in the simulation of deposition [5] and etching [6]. Realistic 3D geometries need to be resolved with a large number of triangles, which then define the masks and layers e.g. for the simulation of ion implantation and lead to large CPU times of some hours on a standard PC. For this work our 3D ion implantation simulator [7] has been accelerated by a factor of about

ten via introduction of an additional floating tensor mesh in the implantation kernel to allow for the fast and accurate simulation for arbitrary triangulated surface meshes and unstructured bulk meshes. Process simulation was started in 2D using DIOS [4] and expanded to 3D before the full 3D simulation of critical process steps. For 3D device simulation DESSIS [4] from ISE AG has been used.

3 Examples

In the following, influences of the variation of key technological parameters are investigated by simulations. The reference device is a triple-gate FinFET with 50 nm gate length and fin width, manufactured in a 50 nm SOI silicon film. The FinFET process includes the thinning of the SOI silicon layer to about 50 nm thickness. However, there are process induced variations of this thickness. As first example, Figs. 1 and 2 show the results of 3D simulation of FinFETs with a silicon thickness of 50nm and 60 nm, respectively.

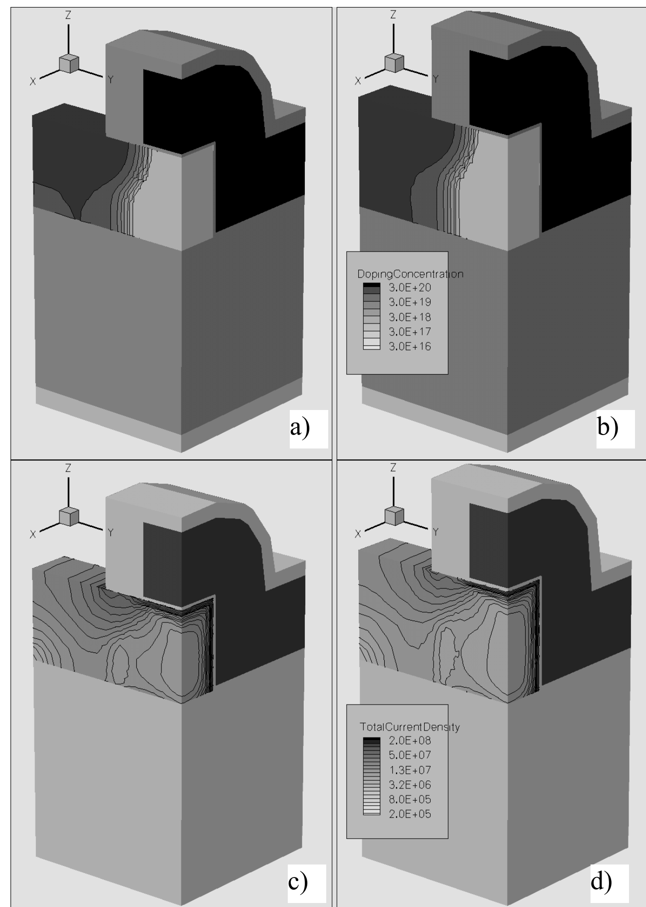

Fig. 1: Simulation of NMOS FinFET transistors with 50 nm (a,c) and 60 nm (b,d) thickness of the silicon film. One quarter of the transistor is shown. a) and b): dopant distribution; c) and d): drain drive current density in A/cm^2

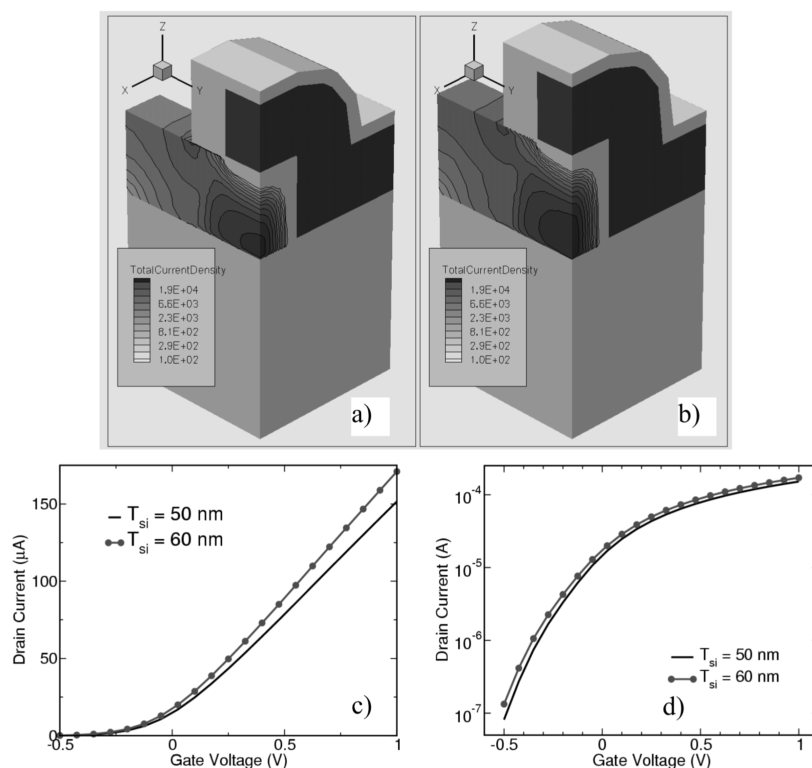

Fig. 2: Simulation of NMOS FinFET transistors with 50nm (a,c) and 60 nm (b,d) thickness of the silicon film. a) and b): leakage current density in A/cm^2; c) and d): transfer characteristics in linear and log scale, respectively

Whereas for the distribution of the dopants in Fig. 1 a) and b) and of the drive current density in Fig. 1 c) and d) only the active domain is extended proportional to the silicon layer thickness, the leakage current (at V_G = -0.5 V, V_D = 1 V) is significantly increased for the 60 nm FinFET as shown in Fig. 2 a) and b), because the domain with high leakage current covers a larger fraction of the cross section for the 60 nm fin. The transfer characteristics displayed in Fig. 2 c) and d) prove this effect: A 13% increase of the drive current and a 60% increase of the leakage current for the 20% increase of the silicon thickness. This means that the control of the silicon thickness is especially important for the leakage current which flows in the bulk, see Fig. 2 a) and b), whereas the drive current flows close to the surface, see Fig. 1 c) and d), and scales with approximately twice the fin height plus the fin width.

Second, the influence of the S/D doping profiles on the performance of the FinFET has been studied. This is especially important for PMOS because of the large implantation depth and high diffusivity of boron. 3D simulation studies show that a very low thermal budget e.g. in a spike anneal is needed. Fig. 3 shows the doping and current distribution in a PMOS FinFET after spike annealing. Fig. 4 depicts the transfer characteristics for two different spacer widths. A change of spacer width by 1/6 affects the S/D profile strongly enough to change the drive current by 66%, and leakage current at V_G = 0.5 V even by a factor of 12.

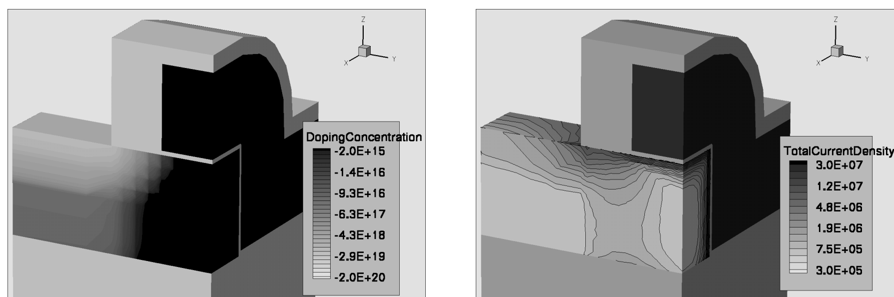

Fig. 3 : Doping (left) and current distribution (right) in a PMOS FinFET

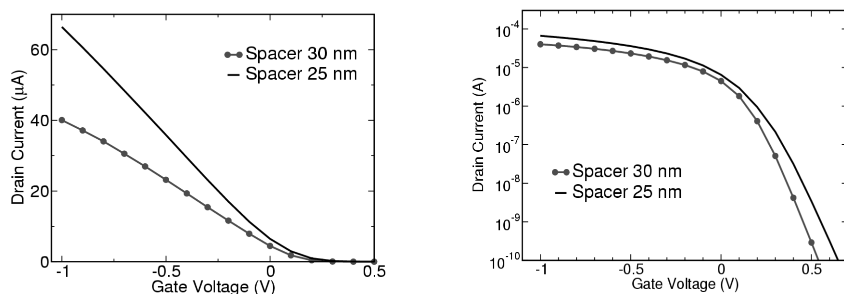

Fig. 4: Transfer characteristics of a 50 nm PMOS FinFET for 25 and 30 nm spacer widths in linear (left) and log (right) scale

4 Conclusion

FinFETs are a very promising device architecture for the next technology generations. Their behavior is dominated by 3D effects which therefore require 3D process and device simulation to optimize device performance and estimate the effects of process fluctuations. An enhancement of 3D process simulation has been presented together with applications.

Acknowledgement

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