An Accurate and Comprehensive Soft Error Simulator NISES II

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Abstract

The authors report an accurate and comprehensive soft error (SE) simulator NISES version II, which includes effects due to cosmic ray high-energy neutrons, thermal neutrons, and α - particles. NISES II covers SE analysis of DRAM, SRAM, and latch (or FF) circuits and it is also applicable for SE analysis of SOI circuits.

1 Introduction

As the device density increased in VLSI, the SE has become a serious problem especially for SRAM and logic circuits [1]. SE simulations are indispensable to estimate soft error rates (SERs) at the circuit design stage and an accurate and comprehensive SE simulator is strongly requested. We report an SE simulator NISES (Neutron-Induced Soft Error Simulator) version II, which is the most comprehensive one among SE simulators previously reported [2-6].

NISES was originally developed for analysis of secondary cosmic ray high-E neutron-induced SEs [3,4]. In NISES II, an accuracy of SER estimations is remarkably improved and, at the first time, it includes effects of thermal neutrons as well as high-E neutrons and α -particles, and also includes bipolar effects of SEs in SOI circuits. NISES II covers SE analysis for DRAM, SRAM, and latch (or FF) circuits.

2 Outline of NISES II

The sources of SEs are high-E neutrons, thermal neutrons, and α -particles (Fig. 1) [1,7]. High-E neutrons and thermal neutrons induce SEs through neutron-nucleus reactions in the silicon substrate and thermal neutron capture reactions of ^{10}B in BPSG (borophosphosilicate glass), respectively.

Figure 2 shows the outline of NISES II. The device structure is the input data. Neutron-silicon reactions, $^{10}B(n, \alpha)^{7}Li$ reactions, and α -particles are randomly generated in the silicon substrate, BPSG, and source materials using a Monte Carlo procedure. If the charged particle passes through a charge-collected region, the charges induced in the region are calculated. We assumed that when these charges pass a critical charge Qc, an SE occurs.

The nuclear reaction database for high-E neutron-induced SEs, was updated by using AMD-V [8], which is modified version of AMD (Antisymmetrized Molecular Dynamics). Estimation method for dimensions of the charge-collected region and for Qc were improved by using device and circuit simulations. Bipolar effects of SEs in SOI circuits were also included in NISES II.

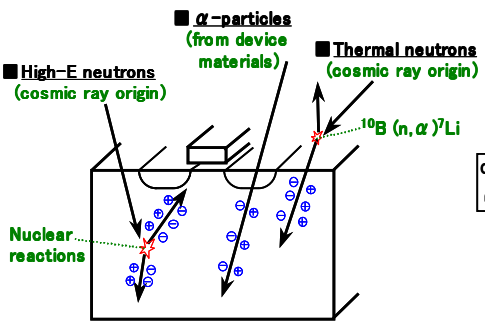


Figure 1: Sources of soft errors.

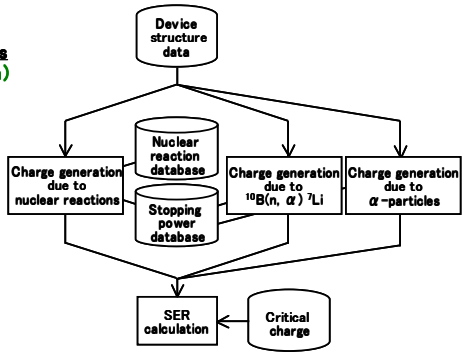


Figure 2: Outline of NISES II.

3 Applications

Accurate estimations of multiple-bit SEs are important for the ECC (Error Correction Code) design [9]. Figure 3 shows high-E neutron-induced multiple-bit SEs in 16Mb DRAMs. Results of NISES version I and version II ware compared with data measured at Los Alamos National Laboratories using a pulsed neutron beam, which has an energy spectrum similar to that of atmospheric neutrons. Accuracy of multiple-bit SERs was remarkably improved, because accuracy of nuclear reaction data for heavy recoil ions is improved in new database. The simulated SERs agreed with measured SERs within a factor of 2 for all multiplicity.

Figure 4 and 5 show accelerated α- and neutron- SERs in SRAM with 0.13 μm technology. α-accelerated tests were performed using ^{241}Am and neutron-accelerated tests were performed at RCNP (Research Center for Nuclear Physics, Osaka Univ.), using a 135 MeV quasi-mono energy neutron beam. Simulated SERs agreed with measured SERs within 20-40% errors. An accuracy of SER estimations of the original version of NISES was within a factor of 2-5 [4]. Therefore, the accuracy is improved in NISES II.

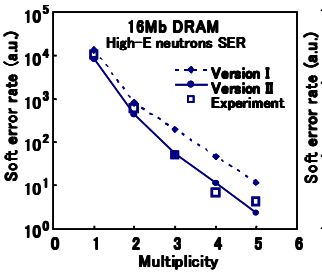
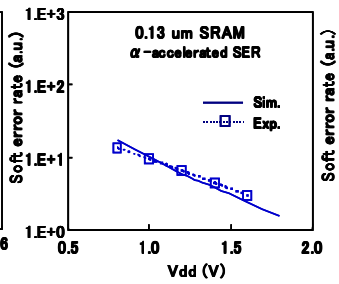


Figure 3: High-E neutron induced multiple-bit SERs in 16Mb DRAM.



Figu re 4: α-accelerated SERs in 0.13 μm SRAM.

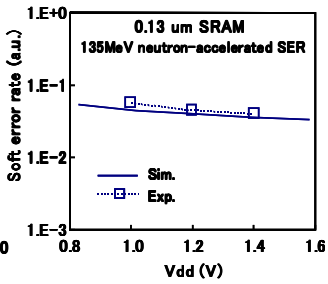


Figure 5: 135 MeV neutron-accelerated SERs in 0.13 μm SRAM.

Figure 6 shows simulated ratio of SERs in 0.18 μ m SRAM with BPSG. About 87% of SER is due to thermal neutrons. However, because the CMP process is used in place of BPSG in recent CMOS technologies, we can ignore the effect of thermal neutrons in most cases. Figure 7 shows the estimated SER trend in SRAMs as a function of technology node. We assumed an atmospheric neutron spectrum and an α -emission rate of 0.001 /cm^2/hour (typical value for material, for examples, mold compound, low- α SnAg bump and etc.). Currently, SERs due to α -particles are similar to those due to high-E neutrons. The SRAM SERs for single cell have similar values in recent technologies, which is consistant with ref. [1].

Because SOI devices are candidate for the solution in future VLSI, SE simulations for SOI circuits are important. When a charged particle hits the channel region in an SOI MOSFT, collected charges remarkably increases due to bipolar effects (Fig.8) [10].

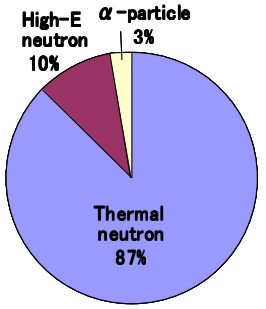


Figure 6: Simulated ratio of SERs in 0.18 μ m SRAM with BPSG.

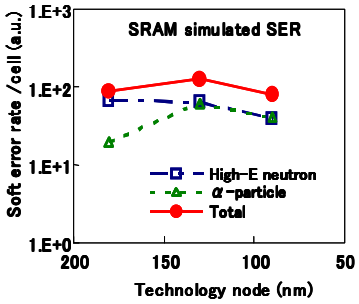


Figure 7: SER trend in SRAMs.

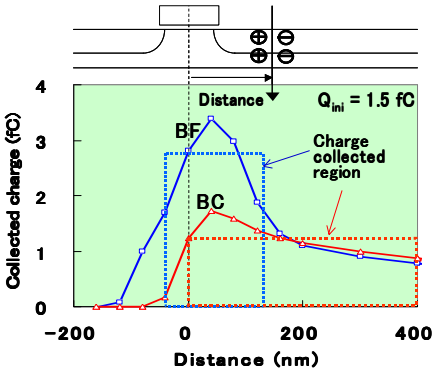


Figure 8: Bipolar effect induced by a charged particle and the charge-collected region in an SOI MOSFET.

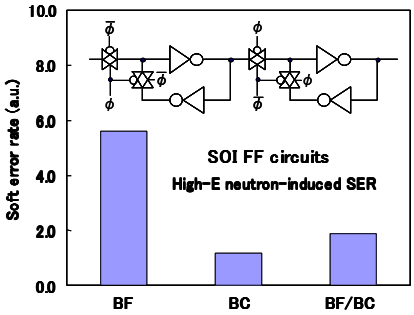


Figure 9: High-E neutron-induced SERs in SOI FF circuits.

A charge-collected region is determined by using device simulations and critical initial charge Q_0c (charges induced in the channel region, $Q_0c < Qc$) is determined by combination with device and circuit simulations. Figure 9 shows high-E neutron induced SER in SOI latch (or FF) circuit. SER with floating body (FB) structure is larger than that with body contact (BC) due to bipolar effect. SER with FB/BC mixed structure is slightly larger than that with BC. FB/BC mixed structure is one of solutions to decrease both SER and cell area.

4 Summary

The most comprehensive SE simulator NISES II includes effects of thermal neutrons as well as high-E neutrons and α-particles, and also includes bipolar effects of SEs in SOI circuits. NISES II covers a wide range of SE analysis for DRAM, SRAM, and latch circuits with high accuracy.

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