Simulation of Lithography-caused Gate Length and Interconnect Linewidth Variational Impact on Circuit Performance in Nanoscale Semiconductor Manufacturing

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Abstract

As the critical dimension (CD) is scaled into nanometer dimensions, operating frequencies exceed a gigahertz, and more functional blocks are added into systems on chip (SoC), interconnect has become a bottleneck in achieving the system performance [1]. In addition, scaling increases the impact of systematic intra-die CD variation (gate and metal linewidth variations) and this variation interacts with the circuit design by degrading circuit speed [2]. One major source of CD variation is the optical lithography process [3]. To determine how the lithography variation impacts circuit performance, this paper introduces a method to incorporate the lithography-caused interconnect linewidth variation in timing simulation. ISCAS benchmark circuits are used to evaluate the circuit performance impact of each optical effect.

1 Introduction

In the nano- and GHz- era, interconnect is a big issue [1] and scaling increases the systematic intra-die CD variation [2]. One major source of CD variation is the optical lithography process [3], including the proximity effect, Coma, lens aberrations, and flare. Variations caused by optical lithography are corrected through mask engineering, including optical proximity correction and dummy feature insertion. These techniques drastically increase the size of the layout database, complicating both tapeouts and the mask generation process. Clearly, feature insertion during mask engineering should be minimized to the extent possible without sacrificing chip performance and yield.

Previous work has studied the impact of variation from optical lithography on transistors [3], [4], and chemical mechanical polishing (CMP) on interconnect [5]. However, most previous tools have had a limited ability to analyze larger scale industrial chips. In our previous work [3], we developed a timing simulation tool which analyzed the relationship between circuit speed and imperfections in lithography. Our previous work focused on the gate layer only. In this paper we have extended our tool to study interconnect linewidth variation. Our tool is applied to ISCAS benchmark circuit [8] and the impact of the gate length and interconnect linewidth variation on the circuit performance is analyzed.

2 Simulation Flow

Our simulation flow in Figure 1 is similar to the previous one except that the interconnect effect is included. The inputs of the tool are the circuit layout information for gates and interconnects in timing critical paths and models of the impact of the proximity effect, Coma, lens aberrations, and flare on CD. The outputs are the delays of the critical paths, accounting for gate length and interconnect linewidth variations caused by the optical proximity effect, Coma, lens aberrations, and flare.

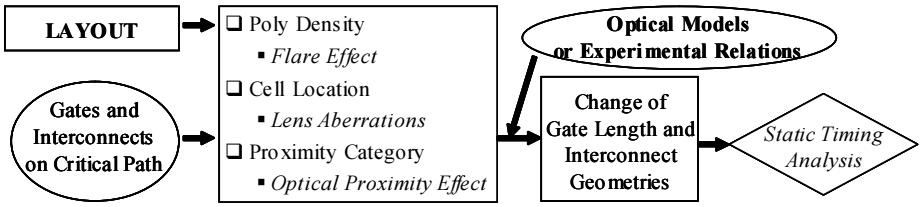


Figure 1: Flow chart.

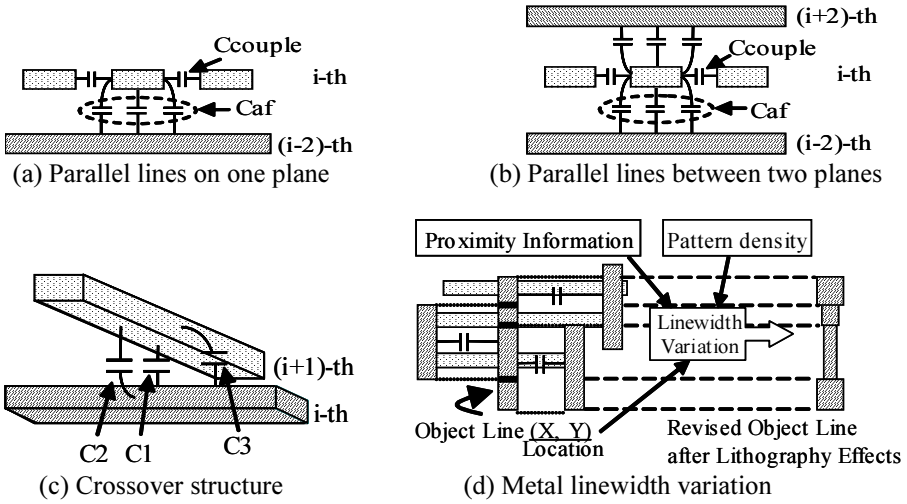


Figure 2: Interconnect structures for the capacitance calculation.

Interconnect parasitic extraction is needed to incorporate interconnect variation in our flow. The conventional extraction methodology of extracting interconnect parasitics requires significant simulation for precharacterization of interconnect. This methodology is not compatible with static timing analysis. Therefore, we have used a more efficient interconnect simulation flow based on Cong's methodology [6] and Wong's analytical capacitance models [7]. According to Cong's five foundations, when the object metal is located in i-th layer, the (i+2)-th and (i-2)-th layers are assumed to be ground and only the electric fields to the closest neighboring metals in i-th layer and the overlapped and underlapped metals in the (i+1)-th and (i-1)-th layers

are considered. The interconnect structure is represented as in Figure 2. The area-fringe and coupling capacitances are shown in Figures 2(a) and 2(b), and the crossover capacitance is shown in Figure 2(c).
Interconnect parasitic extraction inherently includes location and neighborhood information. Therefore, the only additional data needed for our analysis is the pattern density. This is computed by analyzing the layout, as in [3]. Therefore, the analysis of the impact of imperfections in lithography on interconnect CD is achieved by partitioning the metal line based on the neighboring metal patterns and pattern density as shown in Figure 2(d). In our methodology, only the CDs of the interconnect networks in the critical paths are analyzed. However, the CD variation of the neighboring metal influences the coupling capacitance. Thus it is assumed that the neighboring metal CD will match that of the interconnect segment in the critical path in order to save analysis time.

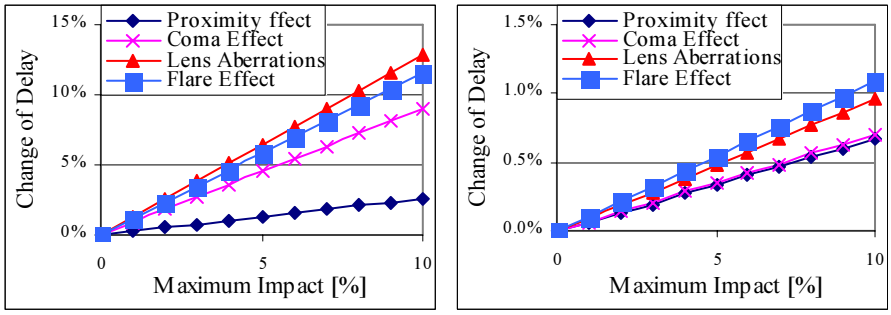
3 Applications

We have applied our methodology to ISCAS benchmark circuit (c7552) [8]. We have investigated the sensitivity of delay to lithography effects (the proximity effect, Coma, lens aberrations, flare). We have varied one of these factors at a time. Each representative characteristic of the optical effects is modeled as in [3]. For the proximity effect, dense patterns are assumed to be larger than isolated patterns. Coma was assumed to cause transistors with dense features on the right to be larger than transistors with the dense features on the left. Lens aberrations were assumed to cause a CD gradient from the left side of the chip to the right. Flare was assumed to cause transistors in dense areas to be larger. The interconnect parameters used in this study are shown in Table 1.

Parameter	Value	Units
Dielectric Constant	3.75	
Metal (Al) Resistivity	3.3	μΩ-cm
Metal 1,2,3 Wiring Pitch	0.5	μm
Metal 4 Wiring Pitch	1.2	μm
Metal 1,2,3 Aspect Ratio	1.5	
Metal 4 Aspect Ratio	1.5	

Table 1: Interconnect parameter.

The impact of each lithography imperfection is shown in Figure 3(a). This result is similar to the results in [3]. In the presence of the proximity effect and Coma, delay is affected by the average CD. In the presence of lens aberrations and flare, delay is a function of the worst case CD. Interconnect variation was analyzed by turning off transistor CD variation. The maximum impact is about 1%, as shown in Figure 3(b). This is much smaller than the transistor impact even though interconnect parasitics increase the path delay by over 70%. The reason is that the impact of CD variation on interconnect resistance is compensated by its impact on interconnect capacitance as shown in Table 2.



(a) Due to transistors and interconnect. (b) Due to only interconnect.

Figure 3: Delay sensitivity when considering CD variations.

Parameter	ΔR/R [%]	ΔC/C [%]
Average	6.7	-1.8

Table 2: Interconnect parasitic RC variation when the flare effect is turned on, and with a range of variation of 10%.

4 Conclusions

Using this simulation flow, we were able to analyze the transistor and interconnect CD variation impact caused by each lithography effect separately. This enables improved targeting of mask engineering. Future work will focus on incorporating models of film thickness variation from chemical mechanical polishing and microloading, combined with the linewidth variation.

References

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