Device performance in conventional and strained Si *n*-MOSFETs with high-κ gate stacks

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Abstract

Based on comprehensive calibration to experimental device characteristics, Monte Carlo simulations have been performed to assess the device performance of sub-100nm Si and strained Si MOSFETs with high-κ dielectrics, with and without consideration of soft optical phonon scattering induced by the introduction of high-κ dielectrics. The impact of interface roughness scattering on the performance enhancement of strained Si MOSFETs has also been evaluated.

1 Introduction

High-κ dielectrics, which reduce the gate leakage current for an Equivalent Oxide Thickness (EOT), are expected to replace SiO_2 at or after the 65 nm node in order to enable further scaling [1]. Aside from the technological issues associated with achieving high-quality high-κ materials, a fundamental drawback of MOSFETs with high-κ dielectrics is the mobility degradation due to strong soft-optical (SO) phonon scattering at the high-κ/Si interface. This scattering mechanism has been theoretically [2] and experimentally [3,4,5] studied and is a fundamental limitation to the inversion layer carrier mobility in such structures. However, to date there has been little quantitative analysis of the impact of this scattering mechanism on device performance.

In this work, we study the impact of soft optical phonon scattering on the performance of sub-100nm conventional and strained Si *n*-MOSFETs using a self-consistent Ensemble Monte Carlo (EMC) device simulator. The effect of the two leading high-κ gate dielectrics, HfO_2 and Al_2O_3, has been examined.

2 Scattering models

Our EMC simulator incorporates all relevant scattering mechanisms including: optical phonon, inelastic acoustic phonon, ionized impurity, interface roughness (IR) and soft-optical phonon scattering. The simulator has been carefully calibrated against transport behaviour in bulk strained Si. The IR model [6] is based on the semi-classical Boltzmann-Fuchs theory, assuming an elastic process and treating interface roughness scattering non-perturbatively by incorporating the effects of scattering as a boundary condition for the Boltzmann Transport Equation. The theory results in the probability of specular and diffuse scattering as a function of the incident solid angle, carrier energy and the autocorrelation function of the rough

interface. We have assumed an exponential auto-covariance function [7] with correlation length, λ, and r.m.s height, Δ. The introduction of high-κ gate dielectrics reduces the gate leakage current typically by orders of magnitude. However, it also introduces strong SO phonon scattering [2]. The scattering results from the strong ionic polarizability of the high-κ material, which is fundamentally related to its large dielectric constant. For low phonon energies, the larger difference between the static and optical permittivities for the two-leading high-κ dielectrics, HfO_2 and Al_2O_3 [2], causes strong scattering of carriers in the inversion layer.

3 Impact of interface roughness scattering

The non-perturbative IR scattering model has been carefully calibrated with respect to the universal mobility curve for Si [8] and corresponding mobility data for strained Si (SSi) [9,10]. We have used a slightly smoother SSi/SiO_2 interface with longer λ [11] in order to achieve agreement with the reported experimental data [10]. The interfaces of the conventional Si and strained Si devices are found to be characterized by Δ=0.5nm and λ=1.8nm, and Δ=0.5nm and λ=3.0nm, respectively.

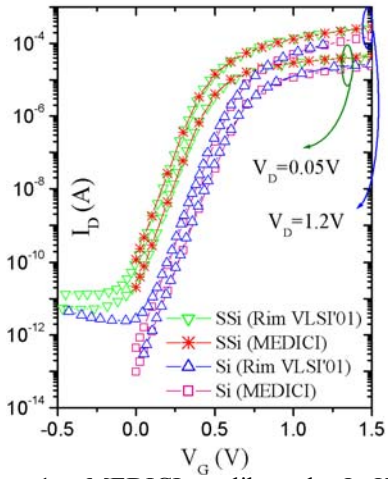

Figure 1: MEDICI calibrated I_D-V_G characteristics of the 67nm *n*-type Si and strained Si MOSFETs.

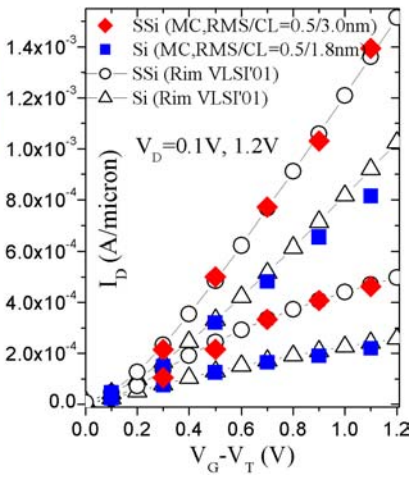

Figure 2: Monte Carlo calibrated I_D-V_G characteristics of the 67nm Si and strained Si MOSFETs.

The test bed for our device simulations are the 67nm effective gate length conventional Si and strained $Si/Si_{0.85}Ge_{0.15}$ *n*-MOSFETs with 2.2nm SiO_2 gate fabricated by IBM [10]. The doping profiles and device structures of these devices have been reversed engineered using MEDICI [12] simulations. The calibrated device information from MEDICI is then used in our self-consistent Ensemble Monte Carlo simulator along with the previously extracted IR parameters for Si and strained Si, enabling us to obtain good agreement between our EMC simulations and the experimental device characteristics without further calibrations. Figures 1 and 2 show the MEDICI and Monte Carlo I_D-V_G characteristics of the 67nm *n*-type Si and strained Si MOSFETs, compared with the experimental data respectively. The reduced IR

scattering for strained Si MOSFETs contributes significantly to the observed performance enhancement for these devices.

4 Impact of soft optical phonon scattering

The calibrated 67nm Si and strained Si MOSFETs have been then used to study the impact of high-κ dielectrics on device performance by replacing the SiO_2 gate dielectrics with high-κ dielectrics (HfO_2 and Al_2O_3) of identical EOT. The same EOT for different gate dielectrics leads to the same gate capacitances and enables identical electrostatic gate control between the devices with SiO_2 and high-κ dielectrics. However, in the presence of high-κ dielectrics, carriers within the inversion layer are subjected to SO phonon scattering, leading to a reduction in the mobility of carriers. Therefore a reduction in device-drive current is expected when high-κ dielectrics are introduced.

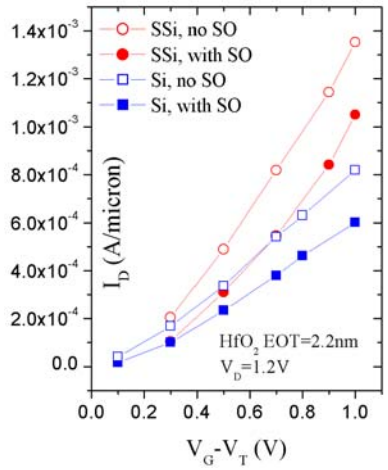

Figure 3: I_D-V_G characteristics with and without SO phonon scattering of the 67nm Si and strained Si MOSFET with HfO_2 gate dielectrics.

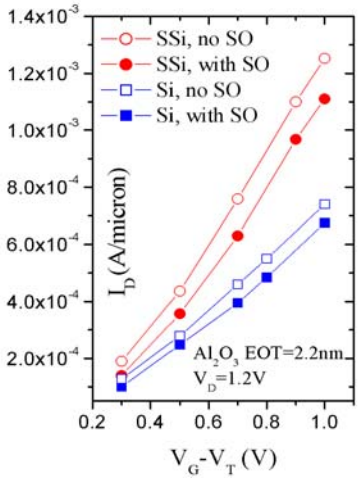

Figure 4: I_D-V_G characteristics with and without SO phonon scattering of the 67nm Si and strained Si MOSFET with Al_2O_3 gate dielectrics.

Figure 3 illustrates the I_D-V_G characteristics for the 67nm conventional Si and strained Si MOSFETs with a HfO_2 gate dielectric. Simulations including SO phonon scattering due to the HfO_2 gate dielectric exhibit a ~27% reduction for conventional Si MOSFET and a ~23% reduction for strained Si MOSFET in drive current I_D at V_D=1.2V and V_G-V_T=1.0V. We observe that devices with a strained Si channel partially compensate for the degradation due to SO phonon scattering. Monte Carlo simulated I_D-V_G characteristics due to the Al_2O_3 dielectric at V_D=1.2V are shown in figure 4. In this case we observe a current reduction of around 10% for both the conventional and strained Si MOSFETs. The smaller current degradations due to SO phonon scattering can be explained by the larger phonon energies and reduction in the difference between the static and optical permittivities [2], as we move from HfO_2 to Al_2O_3. In high-κ gate dielectrics, the large static dielectric constant arises from the

highly polarized ionic bonds, while leading to lower phonon energy and smaller optical permittivity. The conventional SiO_2 has the lowest static dielectric constant, but harder bonds and thus higher phonon energy, which results in the small effect of SO phonon scattering in a Si/SiO_2 based device and we only observe less than 5% reduction in the drive current when applying SO phonon scattering.

5 Conclusions

Ensemble Monte Carlo simulations have been carried out to investigate the impact of interface roughness and soft-optical phonon scattering on the device performance of Si and strained Si MOSFETs. Reduced surface scattering contributes to the observed performance enhancement of strained Si MOSFETs. Significant device current degradations due to SO phonon scattering, of around 25% and 10%, are observed for both conventional and strained Si devices with 2.2nm EOT HfO_2 and Al_2O_3 dielectrics, respectively. Our results indicate that the inherent mobility degradation associated with high-κ gate stacks could be compensated for by the introduction of strained Si channels.

Acknowledgement

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References

[1] International Technology Roadmap for Semiconductors (http://public.itrs.net/), 2003.
[2] M. V. Fischetti, *et al.*, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering", J. Appl. Phys., vol. 90, pp. 4587-4608, 2001.
[3] Z. Ren, *et al.*, "Inversion channel mobility in high-κ high performance MOSFETs", IEDM, 33.2, 2003.
[4] S. Datta, *et al.*, "High mobility Si/SiGe strained channel MOS transistors with HfO_2/TiN Gate stack", IEDM, 28.1, 2003.
[5] W. J. Zhu, *et al.*, "Mobility measurement and degradation mechanisms of MOSFETs made with ultra thin high-κ dielectrics", IEEE Elect. Dev. Lett., vol. 25, pp. 89-91, 2004.
[6] M. Boriçi, *et al.*, "A non perturbative model of surface roughness scattering for Monte Carlo Simulation of relaxed silicon *n*-MOSFETs", J. Comp. Elec., vol. 2, pp. 163-167, 2004.
[7] S. M. Goodnick, *et al.*, "Surface roughness at the Si(100)-SiO_2 interface", Phys. Rev. B, vol. 32, pp. 8171-8186, 1985.
[8] S. Takagi, *et al.*, "On the universality of inversion layer mobility in Si MOSFET's: Part I—Effects of substrate impurity concentration", IEEE Trans. Elec. Dev., vol. 41, pp. 2357-2362, 1994.
[9] J. Welser, *et al.*, "Strain dependence of the performance enhancement in strained-Si n-MOSFETs", IEDM, 31.7, 1994.
[10] K. Rim, *et al.*, "Strained Si NMOSFET for high performance CMOS technology", Symp. On VLSI Tech., pp. 59-61, 2001.
[11] L. Yang, *et al*, "Reduced interface roughness in sub-100nm strained Si n-MOSFETs – A Monte Carlo simulation study", Proc. 5th ULIS, pp. 23-26, 2004
[12] MEDICI Manual, Synopsys Co., 2003.