Numerical analysis for the structure dependence on the subthreshold slope of Floating Channel type SGT(FC-SGT) Flash memory

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Abstract

In this paper, the numerical analysis for the dependence of the subthreshold slope on the diameter of the Si pillar and the length of the overlap region in FC-SGT Flash memory cell is reported. As results, it is demonstrated that FC-SGT Flash memory cell has the steeper subthreshold characteristics than the conventional planar type cell. Therefore FC-SGT Flash memory cell is suitable for the multi-level Flash memory, which requires the steep subthreshold characteristics.

1 Introduction

The spread of the portable equipment such as a digital still camera and a personal digital assistant has accelerated the development of the high density Flash memory. From this viewpoint, Floating Channel type Surrounding Gate Transistor (FC-SGT) Flash memory cell, which has the three-dimensional structure, has been proposed [1]. The FC-SGT structure is shown in Fig.1. The drain, source, and channel region are arranged vertically with respect to the substrate. The tunnel oxide, floating gate, interpoly insulator, and control gate surround the silicon pillar. The program and erase performance of FC-SGT Flash memory cell has been reported in detail [1] [2]. To realize the bi-polarity F-N tunneling program/erase operation [3], for the erase operation, the surface potential of the floating channel region is raised up to the erase voltage due to the carriers generated by (i) the impact ionization in the depletion region, (ii) the band-to-band tunneling in the overlap region between the tunnel oxide and the source, drain region (Fig.2) [2]. Thus the overlap region is necessary to generate the band-to-band tunneling for the erase operation.

On the other hand, as one of the solutions to achieve the high density Flash memory, a great deal of attention has been paid to the multilevel Flash memory. If n denotes the number of bits per cell, the number of the threshold voltage distribution (*VtD*) is 2^n (Fig.3). Therefore it is important to not only produce the tight *VtD*s but also to narrow down the gap between the each *VtD*s (*Vgap*). In the read operation, the control gate is applied to Vread$m$(m=1~2^n-1)(which is the intermediate voltage between one *VtD* and adjacent *VtD*) and the data is determined with the ON/OFF of the memory cell. Thus, it is required that the memory cell has the steep subthreshold characteristics to narrow down the *Vgap,* as the number of bits per cell is increased. However, since it is difficult to improve the subthreshold characteristics in the conventional planar type

Flash memory cell, no attention was almost paid. In this paper, the dependence of the subthreshold slope on the Si pillar diameter and the overlap length (which is needed for the erase operation) is analyzed with the 2D(for the planar type cell) and the 3D(for the FC-SGT type cell) device simulator [4] and discussed.

2 Subthreshold Slope of Flash memory cell

The subthreshold slope of Flash memory cell (S_{flash}) is defined as

$$S_{flash} \equiv \frac{dVCG}{d\log_{10} ID} = \frac{dVF}{d\log_{10} ID}\frac{dVCG}{dVF} \tag{1}$$

where *VF*, *VCG*, *ID* represent the floating gate potential, the control gate voltage, drain current, respectively.

When *S* is defined as $dVF/dlog_{10}ID$, equation (1) is rewritten as

$$S_{flash} = S \times \frac{1}{\frac{dVF}{dVCG}} \tag{2}$$

where *S* represents the subthreshold slope when the floating gate is shorted with the control gate. *S* has been given by

$$S \cong \frac{kT}{q}\ln 10 \times (1 + \frac{Cdep}{Cox}) \tag{3}$$

where k, T, and q represent boltzmann's constant, the absolute temperature, the electronic charge, respectively, and *Cox* and *Cdep* represent the tunnel oxide capacitance, the depletion layer capacitance for the weak inversion, respectively[5]. Also, the *dVF/dVCG* is considered as the sensitivity of the floating gate to the control gate. The *dVF/dVCG* is given by

$$\frac{dVF}{dVCG} = \frac{Cip}{Cip + Cd + Cs + \frac{Cdep}{Cox + Cdep}Cox} \tag{4}$$

where *Cip*, *Cd*, and *Cs* represent the capacitance of the interpoly insulator, the capacitance between drain and floating gate, the capacitance between source and floating gate, respectively. *Cs* and *Cd* is mainly the capacitance of the overlap region(see Fig.1). To improve S_{flash} , it is necessary to decrease *S* and to increase *dVF/dVCG* from equation (2).

First, to decrease *S*, it is important to increase the tunnel oxide capacitance or to decrease the depletion layer capacitance from the equation (3). But for the planar type cell, the depletion layer capacitance tends to increase due to the scaling. Also, it is

difficult to scale down the tunnel oxide thickness because of the data retention characteristics. Thus for the conventional planar type cell, it is very hard to improve S. However for the FC-SGT type cell, *Cdep* reduces to zero due to full-depletion [6], therefore *S* is independent of *Cox*. Thus while keeping the tunnel oxide thickness, FC-SGT Flash memory cell can realize the ideal *S* by decreasing the Si pillar diameter.

Secondly, from equation (4), the high *dVF/dVCG* results from increasing the ratio of *Cip* to *Cox*,*Cd*,*Cs*. The FC-SGT type cell has the larger ratio of *Cip* to *Cox*,*Cd*,*Cs* due to the cylindrical structure than the planar type cell in the same device parameters. But for the FC-SGT type cell, *Cs*, *Cd* may be larger because of the overlap region than the planar type cell which doesn't need the overlap region.

3 Result and Discussion

Fig.4 shows the subthreshold characteristics of the planar type cell and the FC-SGT type cell. The overlap length is 50nm, the drain voltage is 0.05V. The Si pillar diameter is 200nm for the FC-SGT type cell. The rest of device parameters are shown in Table.1. It is found that S_{flash} for the FC-SGT type cell is 74mV/decade and is smaller than that for the planar type cell, i.e. 118mV/decade.

The dependence of the subthreshold slope on the Si pillar diameter and the overlap length for the FC-SGT type cell are shown in Fig.5, respectively. From Fig.5(a), it is found that, as the Si pillar diameter is decreased, the subthreshold slope becomes smaller as expected. Also from Fig.5(b), it is showed that S_{flash} increases by increasing the overlap length. This results from the increase of *Cd*, *Cs* due to the overlap region. But the dependence on the overlap length for the FC-SGT type cell is weaker than that for the planar type cell and becomes furthermore weaker as decreasing the diameter of Si pillar. This feature is caused by the increase of the ratio of *Cip* to *Cox*, *Cd*, *Cs* due to decreasing the Si pillar diameter. This result means that, even if the sufficient overlap region exists for the erase operation, the FC-SGT type cell shows the excellent subthreshold characteristics.

4 Conclusion

We discuss the subthreshold characteristics of the FC-SGT Flash memory cell. The FC-SGT Flash memory cell has the steeper subthreshold characteristics than the conventional planar type cell. By decreasing the Si pillar diameter, the FC-SGT type cell can realize the excellent subthreshold slope even if the sufficient overlap region exists for the erase operation. Thus the FC-SGT Flash memory is suitable for the multi-level Flash memory such as 3bit/cell and 4bit/cell.

5 Reference

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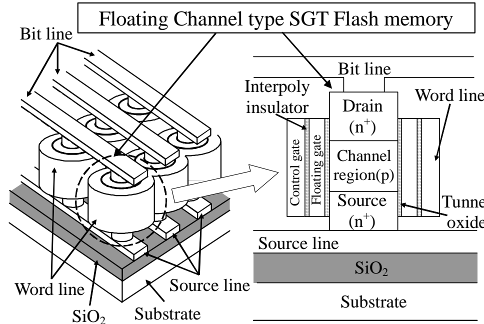

Fig.1: The structure of the FC-SGT Flash memory [1].

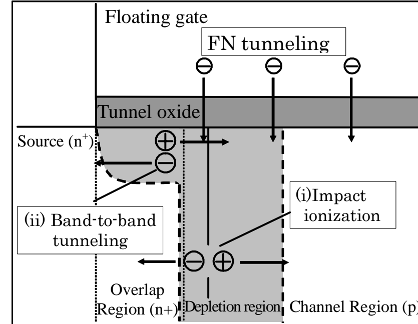

Fig.2: Carrier generation processes during the erase operation [2].

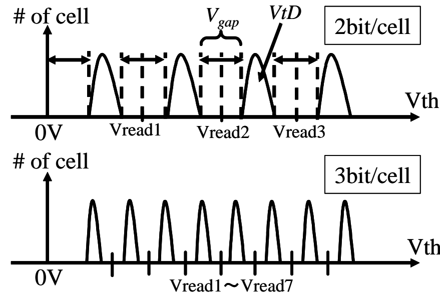

Fig.3: The distribution of threshold voltage for the multi-level Flash memory.

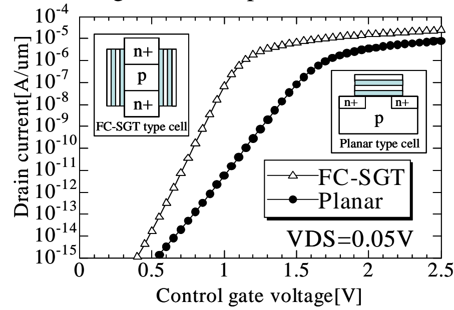

Fig.4: ID-VCG characteristics of the planar type cell and the FC-SGT type cell.

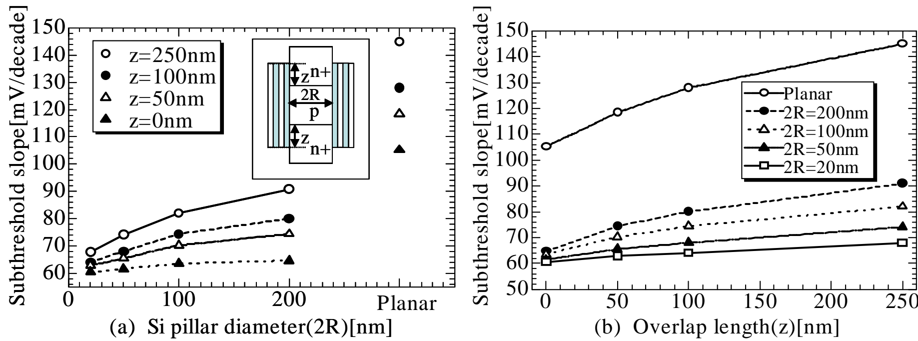

Fig.5: The dependence of the subthreshold slope (a) on Si pillar diameter ($2R$) and (b) on the overlap length (z) between the tunnel oxide and the n-diffusion region for the FC-SGT Flash memory cell and the conventional planar type cell.

Channel Length	**500nm**
Tunnel Oxide Thickness	**7nm**
Interpoly Insulator Thickness	**10nm**
Impurity Concentration of Channel	**1E17cm^{-3}**
Impurity Concentration of Source/Drain	**1E20cm^{-3}**

Table1: The device parameter used in the device simulation.