Analysis and improvments of high frequency substrate losses for RF MOSFETs

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***Abstract*—High frequency substrate losses for RF MOSFETs are analyzed using numerical device simulation. An equivalent circuit model is developed which accurately describes the off-state losses. Based on the model significant improvements in terms of output resistance are demonstrated, using an optimized device on high resistivity substrate.**

Keywords-component; substrate losses, modeling, RF MOSFET

I. INTRODUCTION

It is well known that the silicon substrate affects the high frequency performance of both active and passive devices. For MOSFETs the parasitic resistance from drain to substrate will degrade the efficiency for RF amplifiers, lower gain and f_{MAX} for the device [1, 2]. It has been shown that SOI and high resistivity substrates can improve the high frequency performance of MOSFETs especially the efficiency for RF power devices [1, 3]. For RF-power silicon devices, such as the LDMOS, the general approach is to use epitaxial silicon on a heavily doped and grounded substrate. This paper provides a simulation study of how the substrate affects the high frequency losses for RF-power devices applied on high voltage dual-layer LDMOS. In particular the output resistance (R_{OUT}) in off-state, which has a large impact on the efficiency in power amplifier applications, is studied. The goal is to identify the dominating contributions to the losses, and to investigate how they can be reduced using device simulation and modeling.

II. SIMULATION STRUCTURES

The simulation structure is based on the dual-layer RESURF LDMOS transistor [4, 5], figure 1a. Simulations of the transistor in on-state shows that R_{OUT} in the high frequency region are limited by losses related to the substrate. In fact, these losses are determined by the off-state fundamentals of the device. As the off-state behavior is of great interest, the structure is modified in order to simplify the interpretation of the results. The modified structure, figure 1b, consists basically of two diodes, the source-drain diode and the substrate-drain diode. Consequently, there are two different connections to ground. The simplification removes several effects concerning the source and bulk electrodes. It is confirmed by simulations that R_{OUT}, for different drain voltages, for the simplified structure agrees well with the transistor structure. An additional comparison is made at V_D= 20 V (off-state) with measurement on a transistor and the simplified structure, R_{OUT} is 5.8 kΩ (measured) and 7 kΩ (simulated) and at 5 GHz respectively, W_G=1 mm. It is therefore concluded that the simplified structure accurately represents the transistor in off-state.

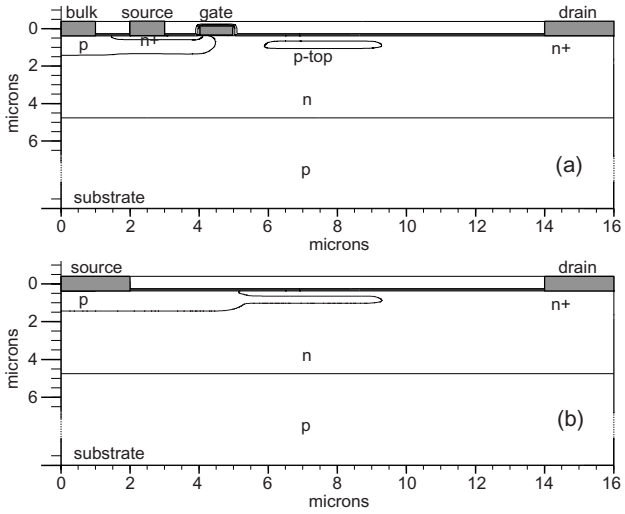

Figure 1. Cross-section of the structures (a) trasitor (b) simplified diode where the former p-top is merged with the p-base.

III. SIMULATIONS

In this study, simulations of the device with three electrodes (or ports), source (s), drain (d) and substrate (sub) are made. The results of the simulations is presented as output resistance $R_{OUT}=[Real(Y22)]^{-1}$ obtained from 2-port data, conductances and capacitances obtained as 3-port data all data is presented for devices with W_G= 1mm.

A. Low resistivity (12.5 Ωcm) epi-layer (10 μm) substrate

From figure 2 it is evident that R_{OUT} for high drain voltages decreases with a constant slope for the entire frequency sweep. As the drain voltage is lower R_{OUT} tends to level out for the highest frequencies. For V_D= 0 V, R_{OUT} is significantly lower and shows a clear leveling out at high frequencies. The constant slope of –2 in the log R_{OUT} vs. log frequency plot indicates that the dominating part can be modeled very accurately with a resistance R_S and capacitance C_S in series. The relation between this series representation and an equivalent parallel resistance R_P, i.e. R_{OUT}, is described by equation 1. Using the equation the results in figure 2 can be interpreted. For high drain voltages the capacitance decreases

due to increased depletion of the n-well, the first term in equation 1 dominates and R_{OUT} is proportional to $1/f^2$. On the other hand, a higher capacitance results from lower drain voltages, i.e. less depletion of the n-well. Consequently, the contribution from the first term decreases and the R_{OUT} decreases. For higher frequencies, the contribution from the first term becomes insignificant compared to the frequency independent second term, R_{OUT} levels out to a value determined by the total series resistance.

$$R_P = \frac{1}{R_s(\omega \cdot C_s)^2} + R_s \quad (1)$$

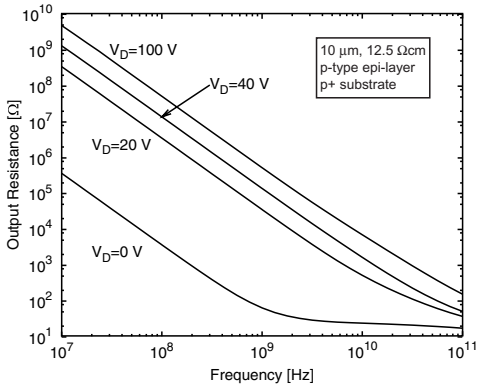

Figure 2. R_{OUT} vs. frequency for structure made on low resistivity epi-layer substrate in off-state at different drain voltages.

The total output resistance R_{OUT} is the equivalent parallel resistance seen from the drain electrode. Obviously, there are two different connections to ground, the path to the source at the surface and the path to the substrate at the bottom. Studying the conductance data in figure 3 reveals their contribution to R_{OUT}. The conductance curves show that the device is limited by the surface region for V_D= 0 V and by the substrate for V_D= 40 V, respectively.

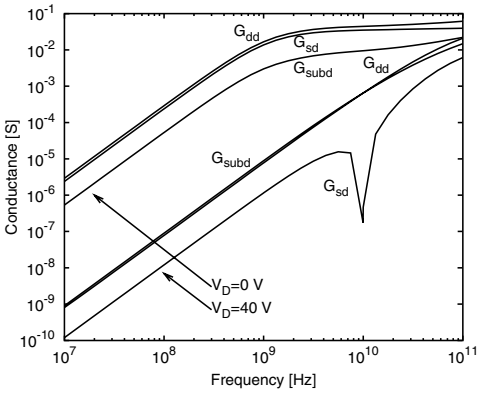

Figure 3. Conductance vs. frequency at V_D= 0 and 40 V.

Even though the source-drain conductance does not contribute significantly to the result for other than low biases, an interesting phenomenon can be seen in the curve. The conductance has a shift in phase at about 10 GHz, a closer examination show that below 10 GHz the source-drain conductance is negative, and therefore reduces the total drain conductance. This phenomenon can be explained by a negative feedback from the substrate to the source. This effect will be fully explained in the modeling section.

B. High resistivity 300 µm substrate

From the results in the previous section it is shown that the connection to the substrate dominates R_{OUT}, except for very low drain voltages. The question then arise how to increase R_{OUT}. One obvious solution is to simply increase the resistivity of the substrate. An attractive result of this is that when the second term dominates, R_{OUT} will be frequency independent, a plateau region is obtained, provided that the substrate connection is dominating.

The same structure as in the previous section was simulated, figure 4, with a uniformly doped substrate with a resistivity of 1 kΩcm and 300 µm thickness. For V_D= 0 V the curve agrees well with the previous case, which shows that the surface contribution is dominating for this substrate as well.

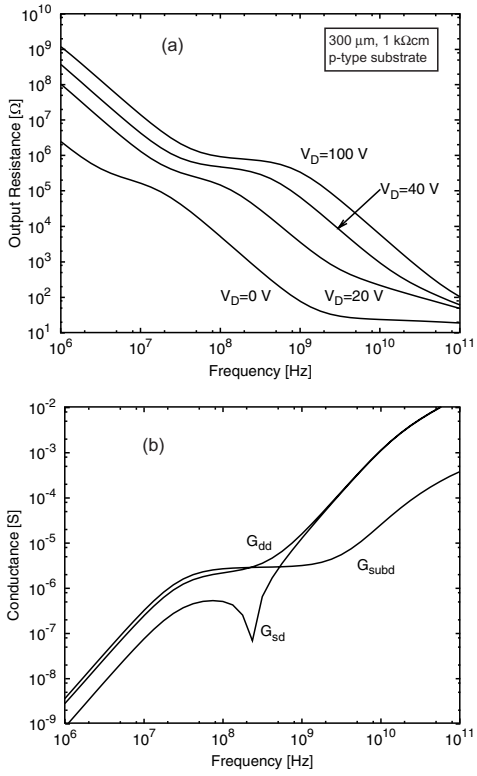

Figure 4. (a) R_{OUT} vs. frequency at different drain voltages and (b) conductance vs. frequency at V_D= 40 V, made on a high resistivity 300 µm substrate.

When a drain voltage is applied, R_{OUT} curve consists of three distinct regions. For low frequencies and up to around 1 GHz, R_{OUT} is significantly lower than for the low resistivity substrate, since the substrate connection is dominating, figure 4b. This is explained by the large increase of the equivalent R_S for the 1 kΩcm substrate, which originates from the undepleted

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part of the substrate. For higher frequencies above the plateau, R_{OUT} decreases due to the contribution from the surface when it starts to dominate, figure 4b, even though the contribution from the substrate has been reduced by a factor of 15.

It is important to note that the actual level of the plateau of R_{OUT} is not correct predicted by equation 1, since it cannot explain the observed voltage dependence. The equation prediction says that the resistance in the frequency independent region will decrease with increased drain voltage, opposite to the true behavior. It is therefore clear that a more complex model of the substrate connection is needed for high resistivity substrates, as will be further discussed in the next section.

IV. MODELING

Using the knowledge about the behavior obtained from the device simulation an equivalent circuit model is proposed, which is partly described in [6, 7], figure 5.

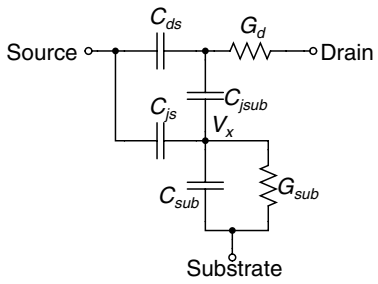

Figure 5. Equivalent circuit model of the device in off state.

The p-n junction between source and drain is represented with the capacitance C_{ds}. The total surface resistance is included in the drain resistance R_d (=1/G_d). C_{jsub} represents the capacitive coupling between the drain and the undepleted substrate. The undepleted part of the substrate is represented with a resistance R_{sub} (=1/G_{sub}) and C_{sub} [1]. The feedback from the substrate to the source is represented by C_{js}. The feedback is only present when a solely capacitive connection exists between the source and the substrate depletion edge.

Model parameters for the structures were extracted from simulated Y-parameter at V_D= 40 V, table 1. The model shows very good agreement with the device simulations in the entire frequency sweep, figure 6. The extracted parameters are consistent with the differences between the structures. The model also describes the voltage dependence correctly, which is related to C_{sub} in parallel with R_{sub}. The model and simulations show further that R_{OUT} is about the same for frequencies at the plateau region and above, if the substrate thickness is reduced to 100 µm. This is of great practical importance for improved heat transportation.

TABLE I. EQUIVALENT CIRCUIT PARAMETERS AT V_D= 40 V.

Device\parameter	C_{ds} [fF]	G_d [mS]	C_{jsub} [fF]	C_{js} [fF]	G_{sub} [mS]	C_{sub} [fF]
12 Ωcm, 20 µm	53	125	120	115	111	1300
1 kΩcm, 300 µm	137	67	20	6.5	$5*10^{-3}$	7

Negative conductances are the result of a capacitance C_{js} over which a complex potential V_x is applied. The source-drain conductance contains of two competitive contributions with different phases. Up to a certain frequency the negative feedback coupling dominates, for higher frequencies the source-drain conductance will change phase due to decreasing imaginary contribution to the potential in V_x, the driving force for the feedback vanish.

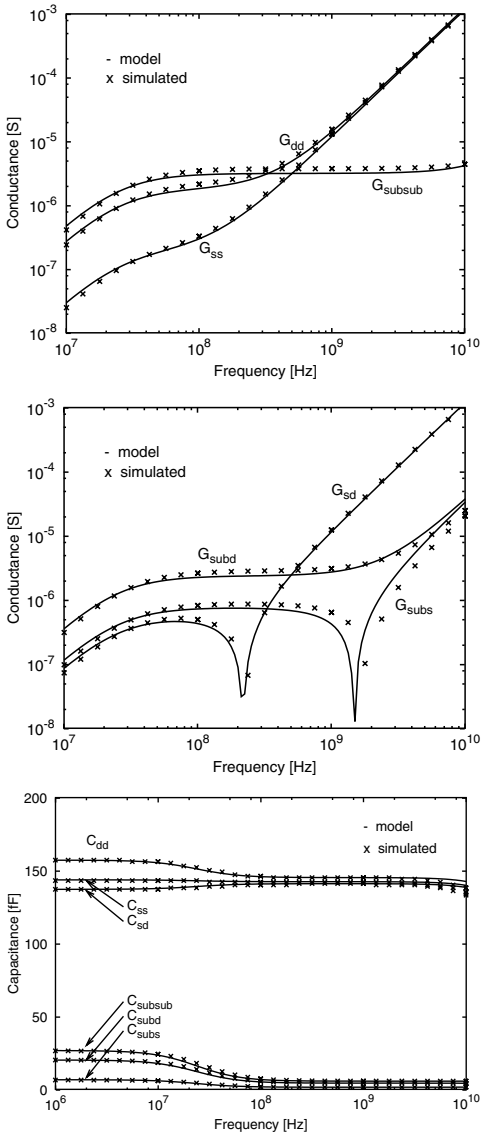

Figure 6. Modeled and simulated conductances and capacitances for the device made on a 300 µm high resistivity substrate at V_D= 40 V.

V. HIGH RESISTIVITY OPTIMIZED SUBSTRATE

The model parameters for high resistivity structure indicate insufficient depletion of the n-well regardless of the substrate thickness. By reducing the total charge and depth of the n-well the surface region will be easier to deplete. These changes in

the n-well result in additional changes of the n- and p-top doses to preserve the charge balance. These changes can have a negative effect on the drain current. Due to the thermal advantages of a thinner substrate, a 100 µm thick substrate was chosen.

R_{OUT} and the conductance at V_D= 40 V are shown figure 7 and the equivalent circuit parameters in table II. One significant distinction in R_{OUT} is the reduced drain voltage dependence for frequencies below 1 GHz. The frequency independent region is enlarged both towards lower and higher frequencies. The substrate-drain conductance has increased for frequencies lower than the frequency independent region. In the frequency independent region R_{OUT} is higher due to larger negative feedback and the frequency where the source-drain conductance starts to dominate has increased towards higher frequencies due to the increased phase shift frequency of the source-drain conductance. In the frequency region above 1 GHz the source-drain conductance become positive for high resistivity substrate and starts to dominate.

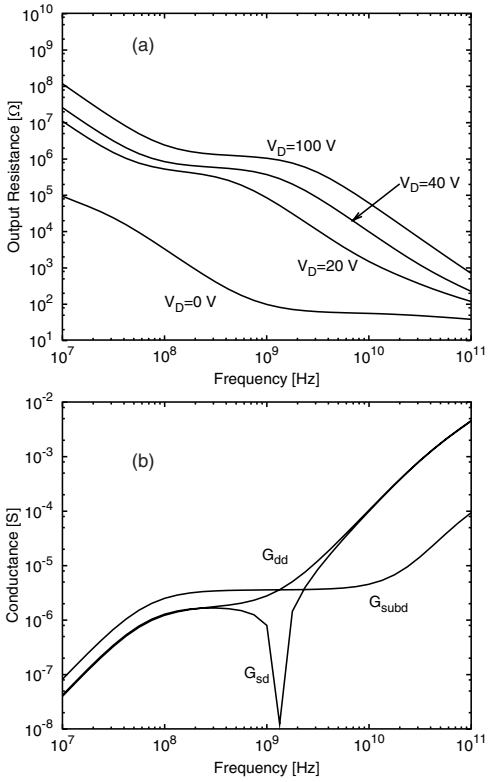

Figure 7. (a) R_{OUT} vs. frequency for different drain voltage and (b) conductance vs. frequency at V_D= 40 V for the optimized substrate.

TABLE II. EQUIVALENT CIRCUIT PARAMETERS AT V_D= 40 V.

Device\parameter	C_{ds} [fF]	G_d [mS]	C_{jsub} [fF]	C_{js} [fF]	G_{sub} [mS]	C_{sub} [fF]
Optimized 100 µm	80	250	17	18	0.028	30

VI. SUMMARY

For the low resistivity epi-layer substrate R_{OUT} was 13 kΩ at 3 GHz and V_D= 40 V for W_G= 1mm. Changing to a 300 µm uniform high resistivity substrate R_{OUT} decreased to 7 kΩ under the same conditions. For the high resistivity optimized substrate device R_{OUT} was improved to 83 kΩ. Compared to the low resistivity substrate device the improvement varied between a factor five and ten for V_D> 40 V at 3 GHz.

The goal was to transform the substrate to minimize its influence on the device performance in the microwave region. Simply by changing the substrate its influence on R_{OUT} was reduced although the device performance suffers by indirectly effects from the substrate on the device. The developed equivalent circuit model, which showed very accurate correspondence with the simulations, was used to study R_{OUT} dependence of the substrate thickness and to design the device made on high resistivity substrate. R_{OUT} was substantially improved and the substrate influence on the performance in the microwave region was eliminated when a drain voltage is applied. The improvement would have been even larger if the surface had not limited the optimized device.

ACKNOWLEDGEMENT

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