INTEGRATED MULTISCALE MULTISTEP PROCESS SIMULATION

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Abstract- We discuss the integration of process simulations for several process steps in the fabrication of a simple Damascene structure. Starting with a blanket silicon dioxide substrate and a patterned mask, we perform simulations of plasma etching, PVD barrier deposition, PVD seed layer deposition, electrochemical deposition of copper using an additive-containing bath, and chemical mechanical polishing. This virtual process sequence demonstrates the use of process simulation to study not just individual process steps, but process flows. After using 2d features and 3d/2d simulations to calibrate models for a particular process, we present samples of fully 3d/3d simulations to show possible approaches to answering questions that cannot be addressed by 2D simulators, such as deposition into dual Damascene structure and the plasma etching of porous materials.

Keywords- process integration simulation, topography evolution, 3d simulation, Damascene process; plasma etching, physical vapor deposition, electrochemical deposition, chemical mechanical polishing, porous dielectric material

I. INTRODUCTION

Fabricating integrated circuits (ICs) is an inherently multi-scale, multi-step, and multi-physics process. The size scales of the units of production (wafers and dies) are centimeters to decimeters, whereas the size scales of the produced structures (devices and interconnects) are micrometers and smaller, and film properties depend on grain and atomic scales. Integrating simulators for these scales [1] is attractive, as it allows self-consistent estimates of wafer scale uniformity and feature scale evolution as functions of position. This can reduce process optimization time and cost.

We show feature scale simulations for the integration of several process steps, in the fabrication of a simple damascene structure, while accounting for the multiscale nature of selected process steps. Starting with a blanket silicon dioxide substrate and a patterned mask, we perform simulations of reactive ion etching (RIE), physical vapor deposition (PVD) of a barrier and a seed layer, electrochemical deposition (ECD) of copper using an additive-containing bath, and chemical mechanical planarization (CMP). These feature scale evolutions can be simulated using EVOLVE [2] which is a feature scale transport and reaction framework. This virtual process sequence demonstrates the coupling of process simulators to study not just individual process steps, but for process flows.

In section VI, we present a 3d/3d process simulation for Ta PVD and plasma etching of porous dielectric substrate, to highlight the roles of '3d/2d' and '3d/3d' (transport/surface dimensionality) topography simulators in 'virtual wafer fabs'. We have developed a simulator that we call PLENTE (parallel level-set environment for nanoscale topography evolution) [3] that uses a multiple level set method to track complex evolving geometries in 3d. EVOLVE is used to determine the distribution of fluxes in these 3d/3d, low pressure transport and reaction studies.

II. PLASMA ETCHING OF DIELECTRIC LAYER

The first step in the virtual fabrication of our demonstration structure is a fluorine-based plasma etch of the silicon dioxide substrate. Inputs to the model are initial geometry, flux distributions and fluxes of the depositing species, and gas-solid interactions. To model the energy distribution of the incoming ion flux, several sub-species of ions are distinguished. Each species is associated with an energy and an angular flux distribution appropriate to that energy, according to a simple sheath model. Similar reactions can be specified for etching of the photoresist mask. This model for transport and reaction during fluorine plasma etching and the associated parameters are typical of process simulations for silicon dioxide etches [4].

We apply this transport and reaction model of RIE to a bank of five openings in a 0.50 μm thick photoresist mask applied to a silicon dioxide substrate, each opening being 0.3 μm wide at the bottom and having sidewalls that open outward, 5 degrees off the vertical. Openings are spaced on a 0.9 μm pitch. We allow the plasma to etch oxide through the mask openings to a depth of approximately 0.8 μm, as shown in Fig. 1 (a). The resulting trenches have vertical sidewalls down to 0.4 μm, and then exhibit a moderate taper, to 0.22 μm wide at the bottom. Over the course of the etch process, there is significant etching of the photoresist mask. Finally, the photoresist layer is assumed to be stripped completely using a post-etch clean.

III. BARRIER AND SEED LAYER DEPOSITION

Simulations of both barrier and seed layer depositions were performed, using long throw PVD and ionized physical vapor deposition (IPVD) respectively. Inputs to these deposition models are initial geometry, flux distributions and total fluxes of the depositing species, and sticking factors. We use the initial geometry provided by the RIE simulation. The sticking factors of the Ta and TaN for the deposition of the tantalum

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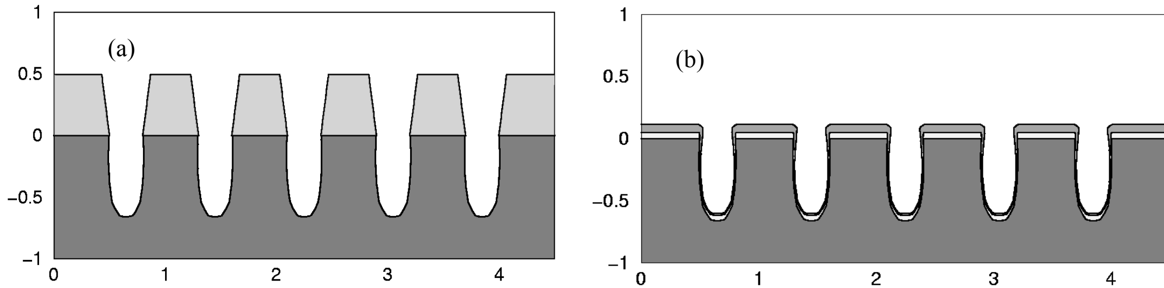

Fig. 1. (a) Feature scale topography of substrate after reactive ion etching to a depth of ~0.6 µm. (b) Topography of substrate after physical vapor deposition of 25 nm TaN, 25 nm Ta and 70 nm copper.

nitride and tantalum barriers were taken to be unity, and we used the metal flux distribution provided in Ref. 5. High energy argon neutrals reflected from the target arrive at the wafer surface with a highly directional distribution (modeled as Gaussian with a 0.2 radian standard deviation) and re-sputter the deposited metal. The re-sputtering model used is based on a yield with a shape given in Ref. 6, with a normal incidence yield that provides an etch/deposition rate ratio of 0,1 on a flat surface. Deposition of the copper seed layer is simulated using an IPVD model given in Ref. 7, with a bias potential of 150 V and a copper sticking factor of 1.0, resulting in an etch/deposition ratio of 16.5% on a flat surface.

Fig. 1 (b) shows the resulting topography after depositing 25 nm each of tantalum nitride and tantalum, and 70 nm of copper to the input structure using PVD, for a total barrier/seed layer thickness of 120 nm on the flats. This thickness on the flats corresponds to a total thickness of 15 nm at the thinnest part of the trench sidewall. This seems quite thin for both barrier and seed layers combined, but highlights the ability of process simulation to determine potential problems with coverage of thin layers.

IV. Electrochemical Deposition of Copper

Following the barrier and seed layer deposition, we simulate ECD of a copper film using a bath containing additives designed to effect bottom-up filling of the trenches. We make use of a feature scale model of "curvature enhanced deposition" from a two-additive plating bath. This model has been shown to reproduce both the bottom-up "superfilling" phenomenon and the production of bumps and elevated areas above trenches [8] exhibited by such baths. The aspect of the model that allows it to predict both superfilling and bumping is the use of an accelerator that adsorbs on the surface and accumulates at a rate that depends strongly on the evolution of local curvature.

Fig. 2 (a) shows a deposition of 0.5 µm of copper (on the flats), into the bank of features, using the seed layer deposited in the previous step. Trenches are completely filled, and the final profile has significant bumps over the mouths of the trenches. The resulting bumps are separate and distinct from one another for this choice of bath and set of process conditions, but this is not always the case for ECD deposits using additives, as shown in Fig. 2 (b) by a simulation over a different set of trenches.

V. Chemical Mechanical Planarization and IMPS

This section presents some details about the IMPS used for modeling chemical mechanical planarization (CMP). Similar methods exist for other process technologies, including chemical vapor deposition [9] and ECD [10]. Common to most of these methods is the performance of a spatial averaging technique, rigorous homogenization in select cases, to turn a small-scale result into a boundary condition for a larger problem. This is the case for our CMP IMPS procedure as well, in which Greenwood-Williamson-like integrals are used to pass information from the asperity scale to the wafer scale. CMP involves complicated solid-solid and solid-fluid interactions [11] that induce boundary lubrication, accompanied by various wear mechanisms between the wafer and the pad, which is very rough by usual tribology standards.

For an externally applied normal load on the wafer of 10 kPa, and a velocity of 30 rpm for the pad and wafer (unidirectional relative velocity of 0.3 m/s at the interface), we calibrate our model to match the observed material removal rate (MRR) of approximately 30 nm/min [12, 13]. Fig. 4 (a) compares the

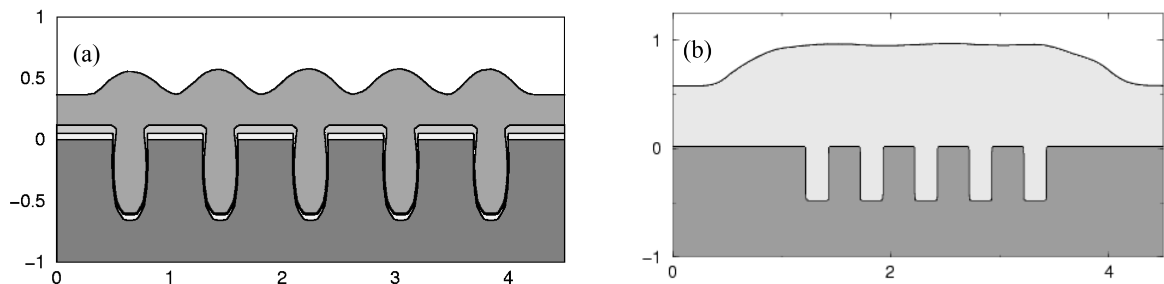

Fig. 2. Feature scale topography after Cu electrochemical deposition using a two-additive plating bath. (a) After electrochemical deposition of 0.35 µm of copper (b) After electrochemical deposition of 0.6 µm of copper with vertical sidewalls and a smaller pitch.

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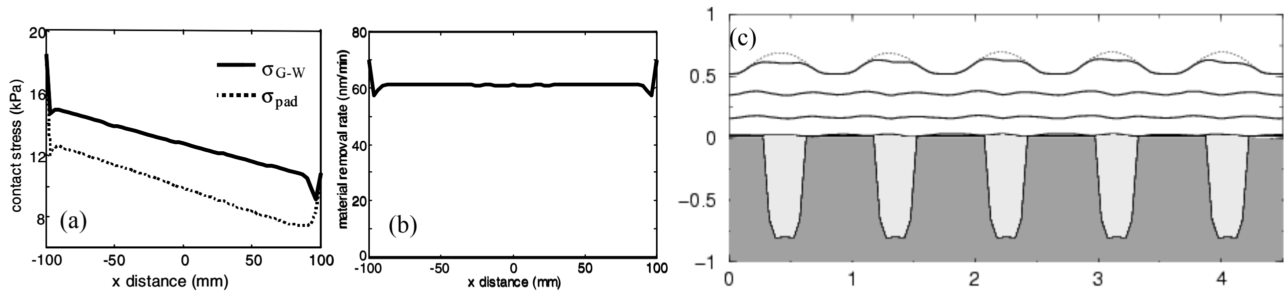


Fig. 3. (a) Contact stress distributions of the bulk pad and asperities (P=10 kPa). (b) Material removal rate (MRR) (P=10kpa). (c) Feature scale topography at center of wafer for several CMP process times.

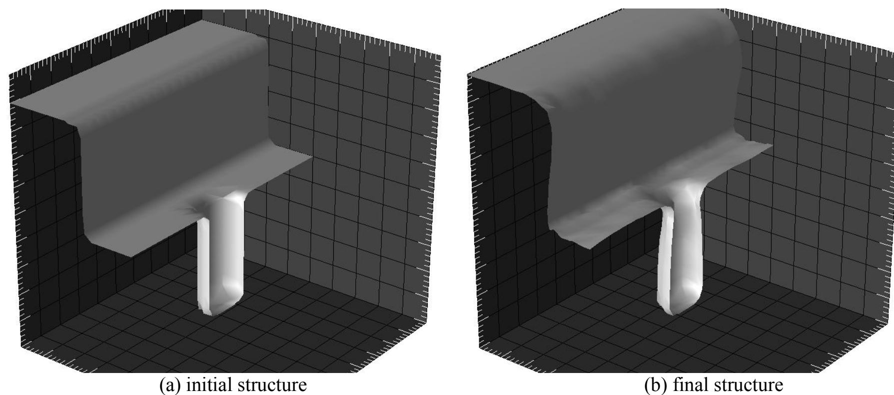
computed asperity contact stresses ($\delta_{G\text{-}W}$) and bulk pad contact stresses (δ_{pad}). At any position on the wafer surface, the slurry pressure is the difference between the bulk pad stress and the asperity contact stress. Sub-ambient pressures are obtained over the entire wafer surface. Fig. 3 (b) shows the MRR across the wafer. ANSYS [14], EVOLVE [2], and the model calibration used to match the experimental MRR on an unpatterned wafer [13] are used to simulate the surface evolution of a set of features, which might result from Cu ECD [8]. Surface removal rates are calculated based on the history of the removal rates and blanket wafer removal rates until breakthrough occurs. Fig. 3 (c) shows the Cu profiles at selected times during CMP, including at the moment of breakthrough to the barrier layer. IMPS as briefly described here will continue to develop, but will have the same overall goal of passing information between scales to achieve consistent solutions. The details of the models used are being improved upon, as most models are or should be, as the understanding of CMP improves.

VI. 3D/3D SIMULATIONS

Substantial insight into a system can be gained using 2d features and 3d/2d simulations to calibrate models for individual process steps and possibly employing a series of these models to examine a process sequence. However, for some applications it is desirable to employ 3d/3d simulations to answer questions that cannot be addressed by 3d/2d simulations. As such, we employ PLENTE to track the evolution of systems in 3d. PLENTE, described in Refs. 3 and 15, is used with the ballistic transport and reaction based process simulator EVOLVE to predict the fluxes and coverages of chemical species on the evolving substrate. A parallel 3D Monte Carlo view factor code is used to calculate transmission probabilities so that EVOLVE may account for re-emission on un-reacted species fluxes between differential surface elements.

Fig. 4 shows a 3d dual Damascene starting structure and a Ta barrier film formed by Ta PVD, using the same surface reaction model summarized above, in a fully 3d simulation using the PLENTE software. The thickness on flat areas is 140 nm. As can be seen in the final profile in Fig. 4 (b), significant bottlenecking can occur and can be made worse by shadowing of the via mouth by the trench walls. Such simulations can be more expensive than their 3d/2d counterparts, but can provide insight into phenomena that may not be apparent or that cannot be studied using lower dimensional representations.

Another application of interest is the plasma etching of porous substrates that are being widely investigated for use as low dielectric constant materials for sate of the art integrated circuit interconnect. Although conventional plasma etching technologies can be used for the patterning of these porous materials, one of the barriers in adapting them to these materials is the lack of the fundamental understanding of how the complicated plasma etching mechanisms interact with the inherently 3D structure of porous materials. Fig. 5 shows a fully 3D simulation study of feature topography evolution using a combination of the EVOLVE and PLENTE software for etching porous dielectric substrates. The plasma



(a) initial structure (b) final structure

Fig. 4. 3d/3d Ta PVD simulation into dual a dual Damascene structure.

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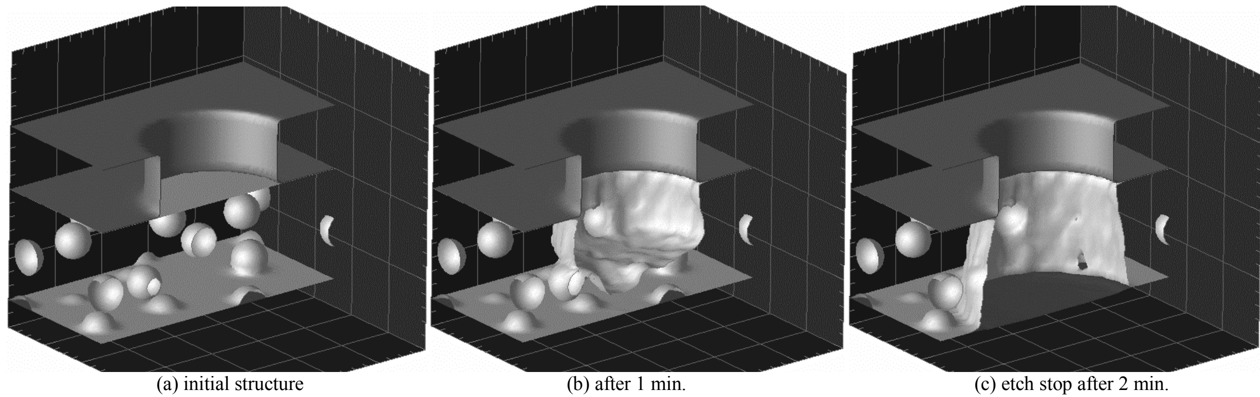

(a) initial structure (b) after 1 min. (c) etch stop after 2 min.

Fig. 5. Reactive ion etching simulation of dielectric material having 0.05 porosity through a 0.5 micron diameter mask opening.

parameters used in experimental data are extracted from assumptions based on simple plasma models. In addition, we use a simple plasma etching kinetic model based on ion-neutral reactant synergism. This is readily extendable to more detailed etch chemistries, as one the strengths of deterministic transport and reaction simulators is the ability to readily handle fairly complex chemistry.

VII. CONCLUSIONS

The fabrication of integrated circuits can be improved by understanding individual process steps [1]. It is also desirable to understand how the individual process steps interact with other steps in the process flow. Simulation of successive process steps can be used as a tool to identify problematic interactions between steps, or to identify and investigate new process sequences. Calibrations of the transport and reaction models will almost always be needed; in general, predictive models are not available and cannot be developed on the time scale on which answers are needed. The resulting empirical or semi-empirical engineering models form the basis process integration studies.

Process integration studies are most useful to study changes in process flows and perhaps process times using well-calibrated engineering models, leaving the process conditions unchanged. For general trends and guidance, it might possible to study the effects of changes in operating conditions and/or consumables. For example, the choice of CMP pads may be influenced by the presence of bumps over the trenches, left by the ECD process. In turn, the bumps may be a result of choosing a particular bath chemistry designed to fill features with a taper similar to the one left by the RIE process. After transport and reaction sub-models have been developed for a given process, those models may be further utilized in 3d/3d simulations to gain insight for situations in which 3d/2d simulations are not well applied. Transport and reaction sub-models limit the accuracy of the predictions of such integrated multistep, multiscale modeling and simulation efforts.

ACKNOWLEDGMENT

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