Oxide Breakdown Model and its Impact on SRAM Cell Functionality

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***Abstract*—The influence of the oxide hard breakdown (HBD) in an SRAM cell on the performance of a circuit that includes the cell, together with the bit select circuit and sense amplifier for the read and write process of the cell, have been analyzed. The analysis of the impact of oxide HBD on this circuit has been performed through the variation of different parameters as the bitline differential voltage and the read and write delays of the cell for different levels of oxide HBD damage in the cell. The results show that oxide BD between gate and source of the NFETs of the SRAM cell seems to have more influence in the circuit performance than in other cell positions.**

Keywords-Dielectric breakdown; oxide reliability; leakage currents; hard breakdown; SRAM

I. INTRODUCTION

Oxide breakdown (BD) may limit CMOS scaling [1], but its impact on circuit functionality is not clear. Oxide reliability models assume that a single BD on a chip will cause circuit failure, but even hard breakdown (HBD), which means the complete loss of the oxide dielectric properties, does not cause complete failure of some circuits [2]. To clarify this controversy, it is necessary to dedicate more studies to analyze the real influence of oxide HBD on circuits. For the moment, the most of the studies have been done on simple structures as capacitors and transistors and very few studies have been done on circuits. In this regard, in this work the impact of oxide HBD on the SRAM cell functionality has been analyzed.

II. DETAILS

The circuit chosen for this investigation includes an SRAM cell, the bit select and the sense amplifier circuit (Fig. 1), although in this work, only oxide HBD in the cell has been considered. SRAM cell (Fig. 3) is a generic circuit (compared to custom logic), and cache memory occupies more than 40% of the chip area. Therefore, by demonstrating that SRAM arrays are relatively insensitive to gate oxide BD, we may realize a significant reliability margin for some chips. The technology of the cells used in this work was 0.13µm/1.2V partially depleted SOI technology [3]. Cell transfer ratios (width ratio of *n*-fet/pass-gate) are chosen to achieve stable cell operation. For SOI technology, it is necessary to consider that increased gate-body current will affect dynamic operation [4]. Regarding to this consideration, in this work we have analyzed for the first time SOI technology taken into account both the gate to body tunneling and the floating body effects.

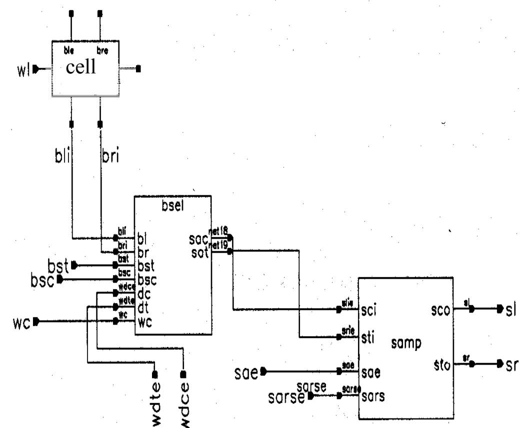

Figure 1: Circuit used to analyze the effect of oxide HBD in the SRAM cell on the performance of a circuit which includes the SRAM cell, bit select circuit and sense amplifier.

In all the transistors of the SRAM cell, only gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situations [5]. Breakdown to the channel can be modeled as a superposition of two gate-diffusion events. Oxide HBD provokes ohmic conduction (I=(1/R)V) through the oxide, and was modeled with simple resistors (value ranging from 10 KΩ to 500 KΩ) between gate and drain or gate and source of the transistors of the circuit (Fig. 2), because we have only considered BD between these points of each transistor. All the possible oxide HBD positions between gate to diffusions of the different transistors of the SRAM cell were analyzed. Just one BD position was considered in each simulation. In order to evaluate the effect on the circuit performance of the oxide HBD in the SRAM cell, the variations (for different HBD resistance values) of the bitline differential voltage (which is the difference between the two bitline voltages developed when the cell is accessed), and

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the read delay and write delays were observed. For comparison of the results obtained from the bitline differential voltage, the static noise margin (SNM) was also evaluated to quantify cell stability [6,7] in the presence of BD at various locations in the cell. The SNM was used to compare the effect of HBD on cell performance with the previous results, although SNM may not be a direct measurement of the BD effect due to the dynamic variation of the beta ratio of the cell and pass transistors.

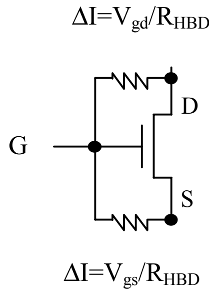

Figure 2: Circuit to model the oxide HBD leakage current from gate to drain or gate to source in a transistor.

III. RESULTS

There are only three topologically distinct breakdown locations between gate and diffusions of the transistors in an SRAM cell, as the one represented in Fig. 3, denoted drain, *p*-source, and *n*-source in the figure. The other possible oxide breakdown locations are completely symmetrical to these ones. Oxide HBD in these positions of the cell (including the pass transistors) were simulated. It has been observed that the oxide breakdown located between gate and source of one of the NFETs of the cell (represented as n-source in Fig. 3) has a greater influence on the cell performance than the other breakdown locations. Oxide HBD in the p-source location does not have appreciable influence on the SRAM cell performance. In the following sections, results about the impact on the cell functionality of oxide HBD between gate and source of one nFET of the cell (n-source), between gate and drain of the cell transistors (drain) and in the pass transistor, as the one represented in figure 3, will be shown.

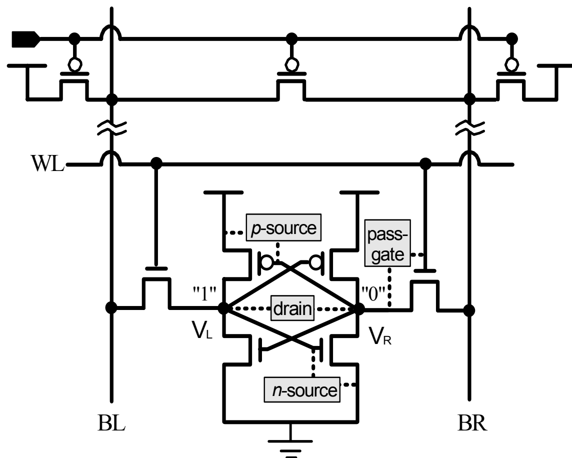

Figure 3: 6-T SRAM cell with possible BD leakage paths corresponding to the cell state shown.

3.1 *Results on bitline differential voltage*

Figure 4 shows the bitline differential voltage as a function of different values of the HBD resistance for oxide HBD in the different locations of the SRAM cell. The bitline differential voltage decreases as the conduction through the oxide increases. There is even a change in sign of the bitline differential voltage, that means a change in the stored value of the cell, for n-source and pass transistor oxide HBD. Fig. 4 shows that n-source oxide HBD is the worst case because the bitline differential voltage starts to decrease before than for the other oxide HBD locations and the change in sign of the bitline differential voltage is produced for higher HBD resistance.

For comparison, the bitline differential voltage is represented in Fig. 5 for the worst case (n-source oxide HBD) when the cell is in the quiescent and opposite state.

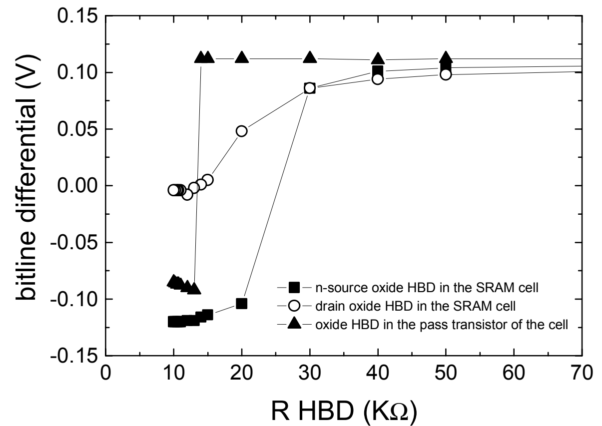

Figure 4. Comparison between the variation of the bitline differential voltage (measured at 50% point of sense amp enable signal) as a function of the oxide HBD resistance for different oxide HBD breakdown positions of the SRAM cell.

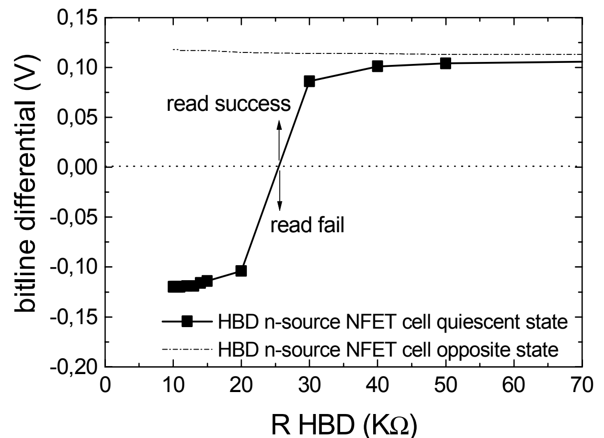

Figure 5: Bitline differential voltage of the SRAM cell in quiescent and opposite state with n-source BD (ohmic) in cell.

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Note that the bitline differential voltage, when the cell is in opposite state, seems not to be affected by the n-source oxide HBD. However, in the quiescent state, the bitline differential voltage decreases as the conduction through the oxide increases and for HBD resistance about 25KΩ the bitline differential voltage changes in sign. This dependence of read success on BD strength correlates well with the SNM results shown in Figure 6. This figure shows the SNM when the cell is in half selected state (word line is pulled high while the bitlines are pre-charged high before the "read" operation), normalized to the SNM of the cell without BD. For the cells considered in this paper, a 50% degradation in SNM results from oxide BD when the current through the BD spot reaches ~20-30 μA at V_{dd} for the worst-case *n* -source breakdown. Pass-gate or *p*-source breakdown may tolerate higher leakage. Fig. 6 shows that for the worst case (n-source oxide HBD) the oxide HBD resistance is ≈25-30KΩ for SNM=0, in agreement with the HBD resistance value for read fail obtained from bitline differential data.

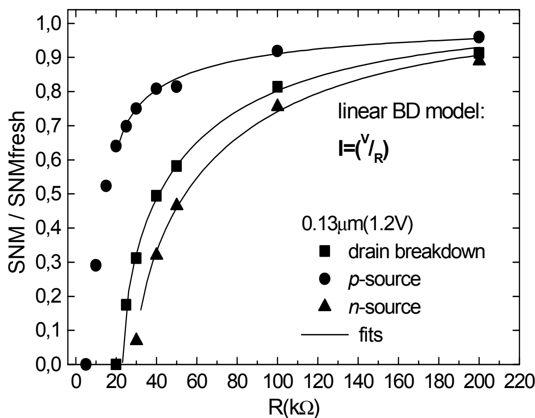

Figure 6: Normalized SNM for HBD as a function of ohmic breakdown resistance R at various locations in the cell.

3.2 Results on read delay

Another parameter to evaluate the effect of oxide BD on the circuit performance is the read delay produced as a consequence of the oxide BD. Figure 7 shows the impact of oxide HBD on the read delay of the stored value of the cell when there is an oxide HBD in the n-source, drain and pass transistor locations. As the HBD conduction through the oxide becomes higher (lower HBD resistance), the read delay increases and abruptly changes for HBD resistance about 25KΩ for n-source oxide BD. The effect of the oxide HBD in other cell locations is not so important, although another abrupt change in the read delay is observed for oxide HBD in the pass transistor of the cell for a HBD resistance of 14 KΩ.

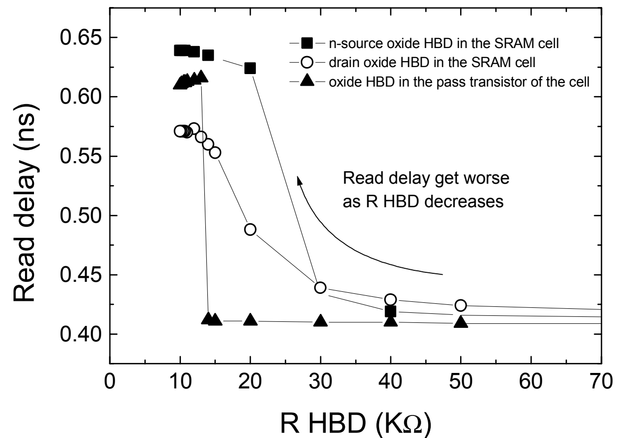

Figure 7: Read delay as a function of oxide HBD resistance in different locations of the SRAM cell. The read delay was measured between the 50% point of the world line signal and the left sense amplifier output during a read operation.

3.3 *Results on write delay*

Figure 8 shows the write delay produced for oxide HBD in the n-source, drain and pass transistor positions of the SRAM cell as a function of HBD resistance. The write delay of the cell decreases as the oxide HBD increases for oxide HBD in the n-source or drain locations. In these cases, for HBD resistance values below 30 KΩ and 20 KΩ respectively the write process of the cell is completely damaged. However, for oxide HBD in the pass transistor of the cell the write delay increases as the HBD conduction becomes higher although for oxide HBD resistance lower than 14 KΩ the write process of the cell is totally destroyed.

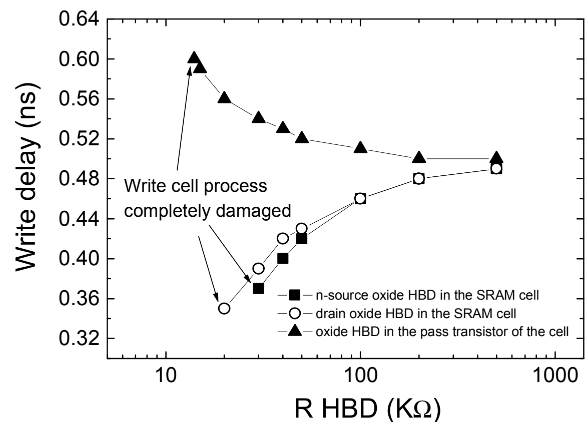

Figure 8: Write delay as a function of oxide HBD resistance in different locations of the SRAM cell. The write delay was measured between the 50% point of the right bitline signal and the value stored in the left node of the cell during a write operation.

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IV. CONCLUSIONS

In this work, an analysis of the influence of oxide HBD in an SRAM memory cell on the performance of a circuit that includes the cell, the bit select circuit and the sense amplifier has been performed. A simple linear model has been used to simulate oxide HBD in the transistors of the circuit. The results show that oxide breakdown between gate and source of the nFET transistors of the SRAM cell is more harmful than in other cell locations. Oxide HBD influences the bitline differential voltages as well as the read and write delays of the cell. The technique used in this work is effectively used to model the oxide HBD impact on circuit functionality and the results give targets for tolerable values of leakage in the SRAM cell caused by gate oxide breakdown.

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