Junction Engineering and Modeling For Advanced CMOS Technologies

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***Abstract*—This paper discusses an integrated modeling approach for diffusion profiles in advanced CMOS technologies. First, for USJ (Ultra-Shallow Junction) arsenic modeling, in addition to a fully-coupled model with implant damage, amorphous layer formation which depends on the Frenkel pair concentration and evolution of {311} defects and dislocation loops based on EOR (End of Range) defects are also used. Secondly, in order to improve polysilicon activation, a hybrid (arsenic + phosphorus) Source/Drain is used for NMOS. We also address the calibration of the hybrid Source/Drain for with various anneal temperatures. It is shown that modeling of the hybrid Source/Drain profile can be achieved by optimization of the dopant's Fermi level dependent diffusivity and the initial value of the point defect concentration in the equilibrium state. Finally, uphill diffusion at low anneal temperature is observed for BF2 USJ and is enhanced with Ge pre-implants. It is caused by a steep interstitial gradient created by preamorphisation and EOR damage, ultra-shallow boron profile, and boron long-hop diffusion [1] [2]. A BIC (Boron-Interstitial Cluster) model is employed to model boron diffusion after a spike RTA at both extension and S/D regions.**

Keywords-implant damage; point defect; shallow junction; advanced CMOS technology

I. ARSENIC SOURCE/DRAIN EXTENSION ENGINEERING AND MODELING

We found that damage does not play a major role for USJ arsenic extension profile modeling [3]. The root causes of the lack of TED (Transient Enhanced Diffusion) are that point defects are removed during crystal regrowth of the amorphous layer and are captured by dislocation loops at the EOR layer. Figure 1 shows the TEM picture of an as-implanted sample and both amorphous and EOR layers are indicated. Based on this picture, the amorphous layer and dislocation loops are implemented into simulation structure by TSUPREM4 (Fig. 2). A good fit to SIMS profiles with a variety of anneal temperatures is therefore shown in Fig. 3 with optimization of Frenkel pair and dislocation loop parameters.

II. HYBRID SOURCE/DRAIN MODELING

A hybrid (Arsenic + Phosphorus) Source/Drain is still a competent candidate for advanced CMOS technologies [4] because it is very useful for reducing junction capacitance and for alleviating polysilicon depletion under tight thermal budget processes. The profile near the arsenic junction becomes graded because of the rapid diffusion of phosphorus inside the highly doped arsenic region. This effect also makes the hybrid junction a sensitive test structure for investigating Fermi level effects on phosphorus diffusion. Phosphorus diffusion modeling is notoriously difficult and embedding the phosphorus profile in a high concentration arsenic layer further complicates the problems. Similar to how we model the extension region, the amorphous layer thickness is implemented into the simulation structure based on TEM pictures. An optimum global profile fitting at different anneal temperatures is therefore achieved by optimization of the dopant's Fermi level dependent diffusivity, the point defects initial concentrations, Frenkel pair and dislocation loop parameters as shown in Fig. 4.

III. BORON SOURCE/DRAIN EXTENSION ENGINEERING AND MODELING

An abnormal uphill diffusion effect [5] is still utilized to make a shallow boron junction. This effect is observed not only for BF2 implant samples but also in boron implant samples with a germanium pre-implant that creates an amorphous layer (Fig. 5) [6]. Because a steep interstitial gradient is created by either BF2 implant or germanium pre-implant and maintained

by chemical-pump effect [2] even when the solid-phase epitaxial regrowth of the preamorphized region is completed, boron diffuses toward silicon surface according to the direction of the interstitial flux. In fact, a time-sequence experiment proves the dopant move in uphill diffusion primarily happens after the crystal regrowth [7]. Furthermore, boron is so close to silicon surface due to low implant energy that they can migrate to it without further interactions with point defects, dopant atoms or the silicon lattice. It implies many boron-interstitial pairs can directly diffuse from the boron tail where the interstitial supersaturation is the highest to surface because of the steep interstitial gradient and the short distance to the silicon surface. It is also verified by simulation with ISE FLOOPS [2]. Because the anneal temperature is another critical parameter to enhance this effect (Fig. 6), a time-temperature matrix experiment is therefore proceeding.

For high activation, an anneal following Solid Phase Epitaxy is still necessary. Due to the BIC behavior, a high anneal temperature and short anneal time are recommended [8]. A spike RTA with a high ramping rate is therefore utilized in order to get the minimum sheet resistance (Rsh) at certain junction depth (Xj). In order to well simulate the boron profiles, BIC model is calibrated with both marker layer [9] and shallow junctions created by low energy implant. Figures 7 and 8 show the simulation results based on the process conditions shown in [9]. The simulations reproduce the 740^{o}C experimental results very well. Furthermore, the BIC model accuracy over a range of anneal temperature is also observed in Fig.9.

IV. Boron Source/Drain modeling

Instead of BF2 which is used in the extension region, boron is used at the Source/Drain for the deep junction. BICs (boron-interstitial clusters) still play an important role in controlling boron TED. A large fraction of the implant damage is clustered into BICs and then forms immobilized boron in high concentrations at the early stages of the anneal. The activation process happens sequentially by cluster dissolution [8]. There is therefore a tradeoff between TED and activation. A well calibrated model can help us to optimize this process. In order to simplify the BIC model, only BI2 and B4I are considered in this model, as small and large clusters respectively. The number of "4" is an empirical fitting result that lumps a variety of BICs into an effective cluster size. A conventional fully-coupled model and {311} cluster are also considered in this model. Figure 10 shows the calibrated result.

V. Two-Dimensional Process Simulation and Devices Characteristics

The diffusion model described above was implemented into Synopsys-TSUPREM4 and validated versus a state-of-the-art CMOS technology with 65nm gate length and 1.6nm oxide [10]. Figures 11 and 12 show that the TCAD model accurately describes the short channel behavior.

VI. Conclusion

We address the technologies used to form both ultra-shallow and deep junctions for advanced CMOS technologies. The physical models that describe the profile evolution are also described. Generally, TEM pictures are used to identify amorphous and EOR layers which are implemented into the simulation structure. A Fermi level dependent diffusivity is optimized to model the hybrid Source/Drain. Up-hill diffusion can reduce boron junction depth and is verified with ISE FLOOPS. A BIC model is necessary for both deep and shallow boron profile modeling after spike RTA anneals. Above engineering are implemented into a state-of-the-art CMOS technology and the calibrated parameters are also included in a two-dimensional process simulation. The simulation result is in good agreement with silicon data.

Acknowledgment

We thank G. Mannino et al. [9] for the share of experimental SIMS data. The data help us demonstrate the calibration accuracy of BIC model in this work. Both the simulation results and SIMS data are shown in Figs. 7 and 8.

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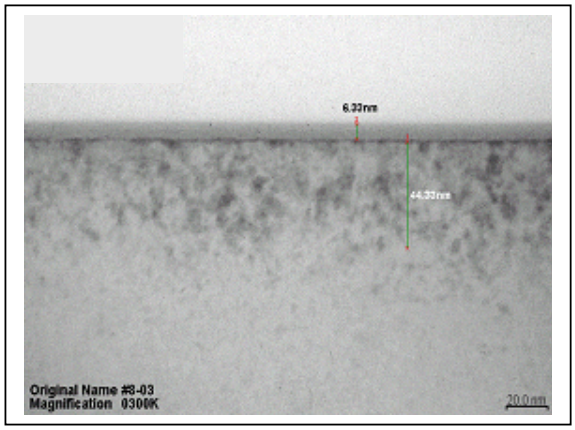

Figure 1. TEM picture with middle dose pocket implant and high dose arsenic implant. Both amorphous and damaged layers are observed.

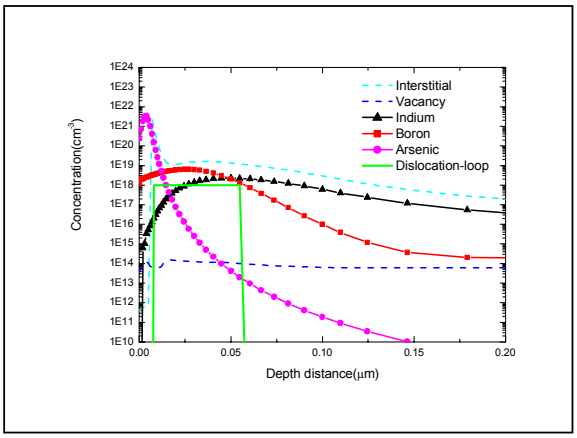

Figure 2. Doping profiles, interstitial, vacancy, and dislocation loops distribution of the silicon shown in Fig.1.

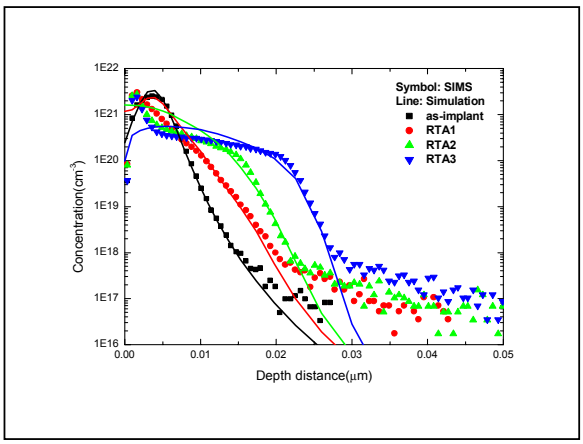

Figure 3. The calibration result of USJ arsenic annealed at a variety of temperature.

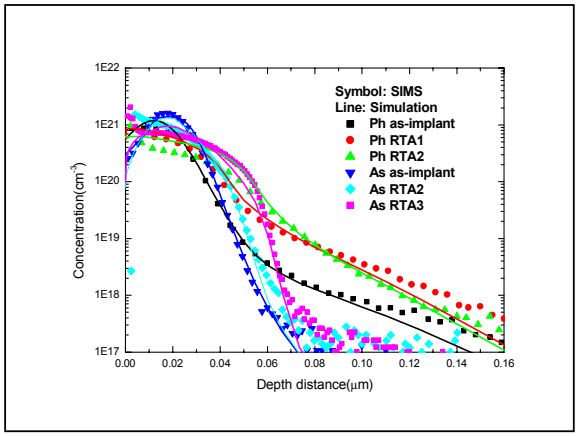

Figure 4. The calibration result of hybrid-NSD annealed at a variety of temperature.

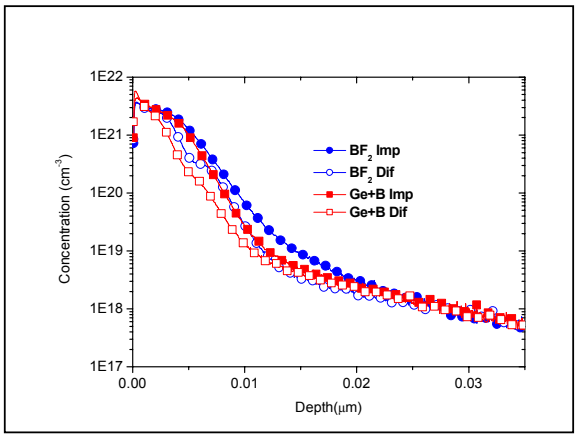

Figure 5. Boron Uphill diffusion is observed at low temperature diffusion (700°C, 2 hours). It is enhanced with Germanium pre-implant.

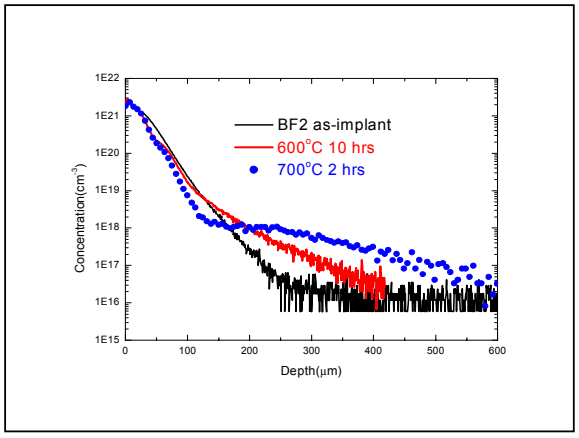

Figure 6. The temperature dependence of boron uphill diffusion. 700°C/2 hours anneal shows more uphill diffusion compared to 600°C/10 hours.

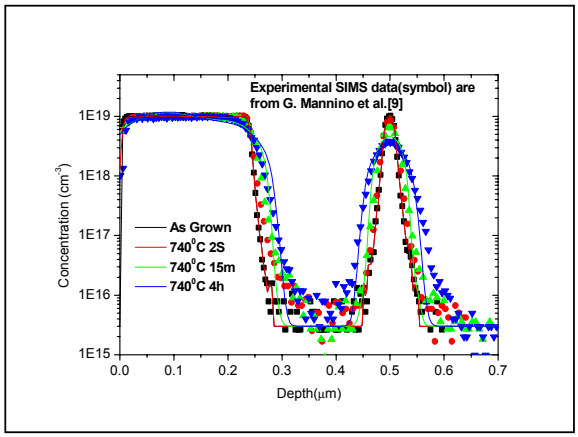

Figure 7. The simulations reroduce the experimental results [9] very well. Silicon/60Kev/2E13 was implanted before the following 740°C anneal.

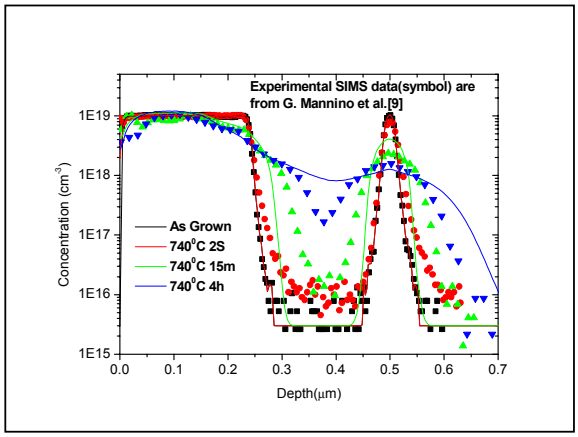

Figure 8. The simulation reproduce the experimental results [9] very well. Silicon/60Kev/1E14 was implanted before the following 740°C anneal.

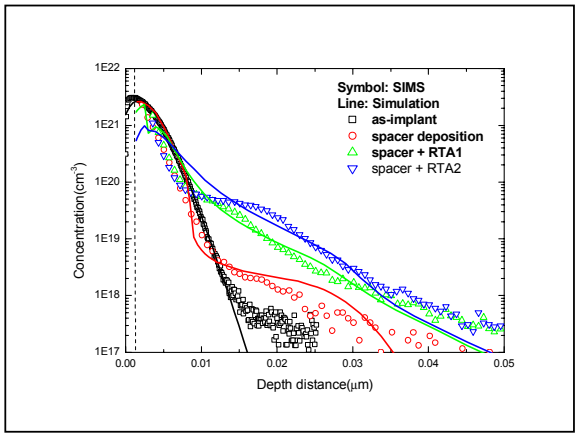

Figure 9. The calibration result of PMOSFET extension BF2 USJ profiles with BICs model.

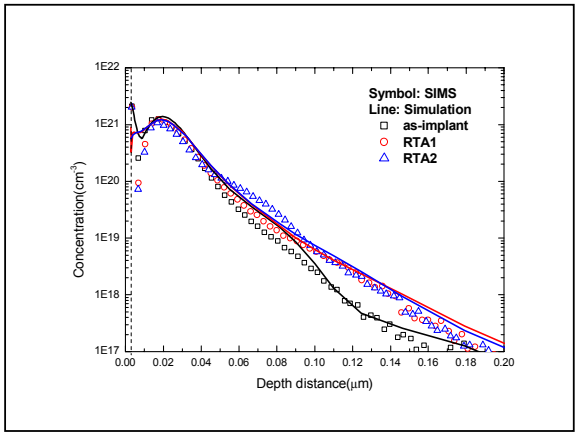

Figure 10. The calibration result of Boron source/drain profiles with BICs model.

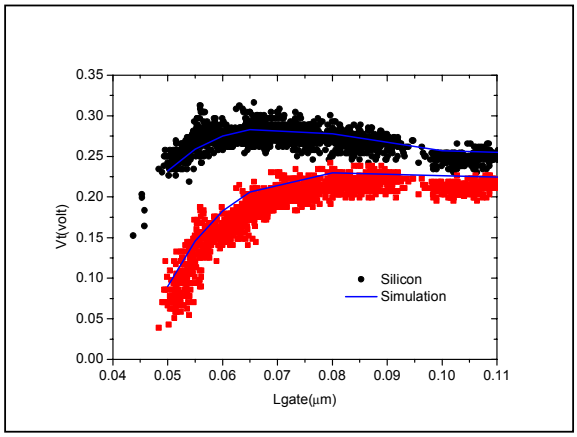

Figure 11. NMOSFET threshold voltage versus Lgate with Vds=0.05 and 1.0 voltage.

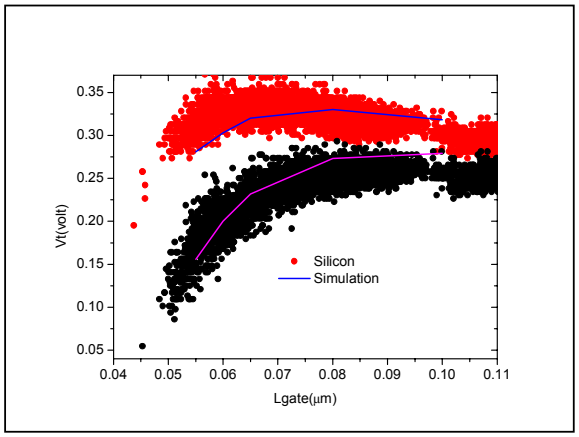

Figure 12. PMOSFET threshold voltage versus Lgate with Vds=0.05 and 1.0 voltage.

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