Optimization of L_{Gate} for ggNMOS ESD protection devices fabricated on Bulk- and SOI- Substrates, using Process and Device Simulation

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***Abstract*— The high- current characteristics of ggNMOS fabricated on bulk- as well as on SOI- substrates using a 0,6 μm-CMOS technology have been simulated for different values of the gate length L_{Gate}. Prior to the simulation, the doping profiles and physical transport parameters were calibrated with reference to measured data. The snapback differential resistance R_{spdiff} is found to be higher for SOI-devices. Also, an optimum value of L_{Gate} is determined for the bulk- substrate, yielding a minimum snapback holding voltage V_H. For SOI fabrication, however, V_H decreases with shrinking L_{Gate}. We explain this behavior on the basis of the electrothermal simulation results.**

I. Introduction

In former work, experimental investigations concentrated mostly on ESD robustness with respect to SOI- technologies (e.g.[1]-[4]). Also, a few predictive device-level simulations have been reported which focus on ESD protection devices fabricated on bulk substrates (as in [5], [6]). However, to our knowledge no study on the optimization of the ESD behavior of protection devices on SOI substrates has been presented so far, which exploits a fully self-consistent electrothermal device model with well-calibrated physical parameters.

II. Calibration of physical parameters

In order to obtain reliable doping profiles, we performed a complete 2D-process simulation sequence, which had been calibrated using 1D data from spreading resistance measurements, for both bulk- and SOI substrates. A 2D-cross section of the device structure is shown in fig. 1. Prior to the ESD simulations we performed a calibration of the physical models with reference to forward- and reverse DC- characteristics of fabricated diodes; in this way we obtained the temperature-dependent values of the carrier lifetimes and the impact ionization parameters. We achieved good agreement with the measured data, as it is shown for the reverse characteristics in fig. 2.

III. Protection device optimization

Our goal was to minimize the value of the snapback holding Voltage V_H for the ggNMOS' high-current characteristics, targeting an effective clamping under ESD stress. To this end,

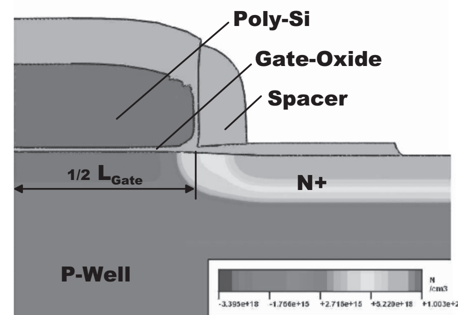

Fig. 1. 2D- doping profile of a ggNMOS as obtained from calibrated process simulation

we simulated the high-current characteristics of ggNMOS devices for several different values of L_{Gate}, using the calibrated 2D-doping profiles and transport parameters and considering both bulk as well as SOI substrates. An overall device width of 400μm and uniform current conduction were assumed. In our calculations, the contact to gate spacings were left unchanged for all values of L_{Gate} (DCGS=SCGS =5μm). As is easily extracted from figs. 3 and 4, the snapback differential resistance is larger for the SOI- devices. This is a consequence of the smaller current conduction area: beyond the snapback point, an increase in the electric field in the base region is necessary for sustaining a larger current density. This translates into a higher terminal voltage for a higher current, where the scaling is controlled by the device dimensions, leading to the observed R_{spdiff}.
For bulk devices, we found a minimum V_H at L_{Gopt} = 1μm, as opposed to the scaling reported in [1], while for SOI technology the smallest value of V_H is obtained for the shortest possible channel, $L_{Gate} = L_{Gmin} = 0,6\mu m$. SOI devices also exhibit smaller values of V_H compared to bulk devices.

IV. Discussion

The notoriously different behavior observed for the two different substrate types investigated, as has been described

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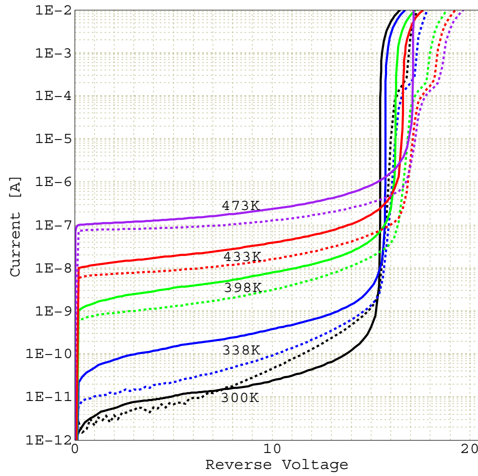

Fig. 2. Reverse characteristics of a pn-diode from the technology investigated; temperature range 300K-473K (● ● ● simulated; —— measured)

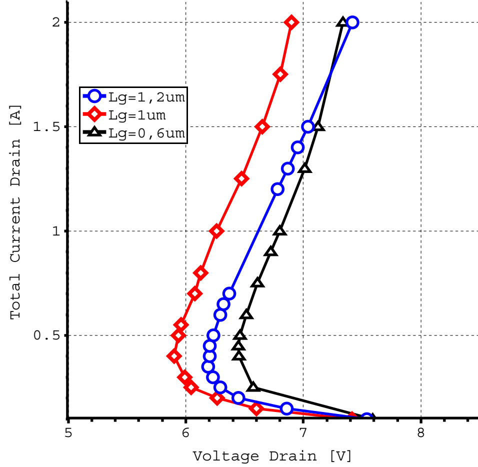

Fig. 3. Simulated high-current characteristics of a ggNMOS fabricated on bulk substrate

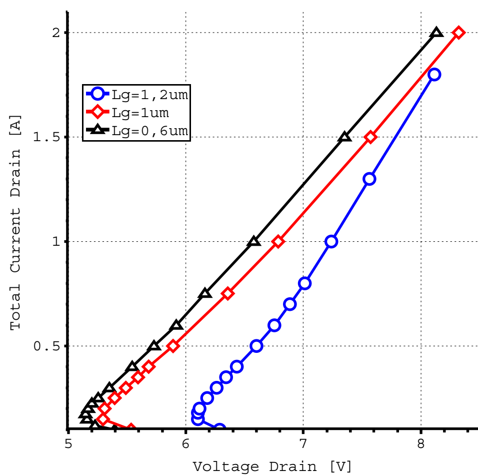

Fig. 4. Simulated high-current characteristics of a ggNMOS fabricated on SOI- substrate

in the foregoing section, can be qualitatively explained as follows:

A. Current spreading

As can be seen in figs. 5 and 6, the current flow during ESD stress in bulk devices is not restricted to the cylindrically shaped portion of the p-Well-n^+-Drain-junction, but instead it spreads out over the whole junction area, conforming with the well-known lateral base widening in BJTs [7]. This current spreading mechanism is limited by the fact that the current density isolines cannot exhibit an arbitrarily high curvature, because from $1/q \cdot \nabla \vec{j_n}] = R$ for stationary currents it follows that the decrease of the $\vec{j_n}$-component normal to the plotted isolines is determined by the recombination rate R in the p-Well. A larger L_{Gate} allows for more effective current spreading, leading to an increase of the device current at a given voltage.

B. Effective base width

On the other hand, L_{Gate} is the effective base width for a substantial portion of the carriers injected into the base; therefore the current gain is expected to decrease with larger L_{Gate}.

These contrarily acting dependencies give rise to the existence of an optimum channel length, L_{Gopt}, for bulk devices, where the target consists in maximizing the terminal current $I = \int\int \vec{j} \cdot d\vec{A}$ at a given fixed terminal voltage, leading eventually to a minimum value of the snapback holding voltage, $V_H min$.
In SOI devices, however, the curvature of the current density isolines is limited by the extension of the silicon layer in the vertical direction, rather than by recombination; therefore, lateral base widening does not have any perceptible effect on the snapback holding voltage. This explains why the device with the smallest L_{Gate} will also exhibit the smallest V_H. The corresponding current density isolines for the transistors with L_{Gate}=0,6μm and L_{Gate}=1,2μm, both at a current I_{sp}=0,3A are shown in figs.7 and 8. Since most of the current flows in horizontal direction, the overall current gain increase due to L_{Gate}-narrowing is stronger than in devices based on bulk technology, and therefore also V_{Hmin} is smaller for SOI devices.

V. Conclusions

We demonstrated the optimization of ESD protection structures fabricated by the use of an industrial 0,5μm-CMOS fabrication process by employing process and device simulations. Devices built on bulk- as well as on SOI substrates were investigated. Physical transport parameters were extracted from measurements of the DC characteristics of real devices. On the basis of the calibrated physical models, accurate electrothermal simulations of ggNMOS- protection structures were performed. We found that these devices exhibit significantly different values of the optimum gate length L_{Gopt}, depending on the substrate material. We could explain this behavior by

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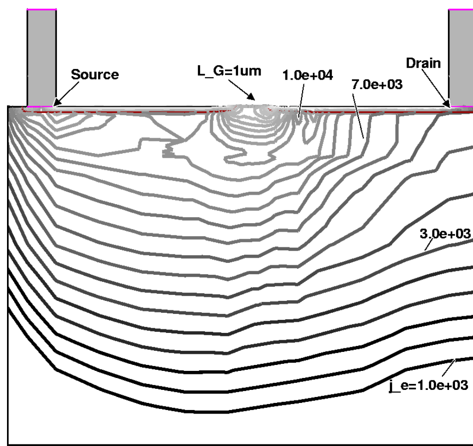

Fig. 5. Current density isolines for a ggNMOS with L_{Gate}=1μm on bulk-Si. Darker lines denote lower current density

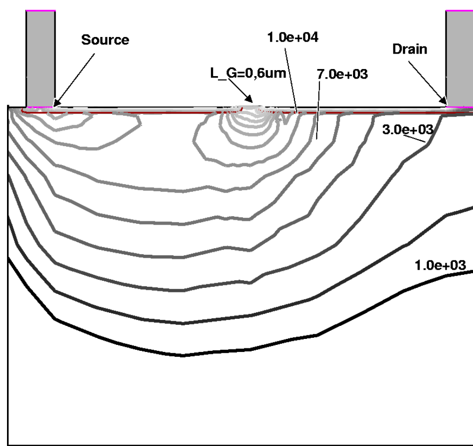

Fig. 6. Current density isolines for a ggNMOS with L_{Gate}=0,6μm on bulk-Si. Darker lines denote lower current density

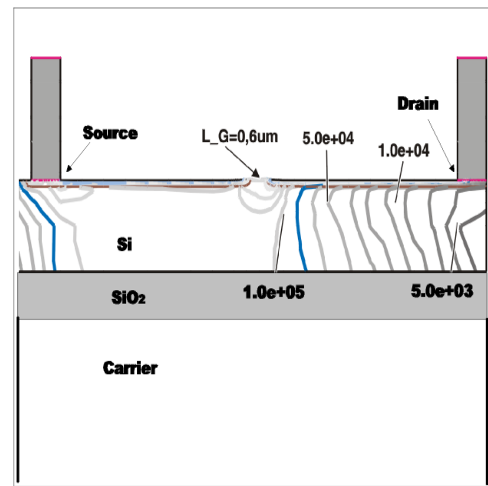

Fig. 7. Current density isolines for a ggNMOS with L_{Gate}=0,6μm in SOI technology. Darker lines denote lower current density

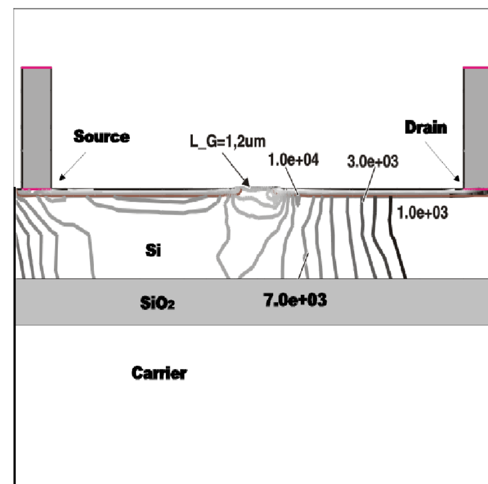

Fig. 8. Current density isolines for a ggNMOS with L_{Gate}=1,2μm in SOI technology. Darker lines denote lower current density

analyzing the current flows as obtained from device simulation and from theoretical considerations.We also found that the decrease of current gain with larger L_{Gate} for the parasitic BJT is the dominant effect in devices fabricated in SOI technology; thus, minimum L_{Gate} should be chosen for this kind of substrate. However,there exists a trade-off with an optimum value of L_{Gate} for devices built on bulk substrates; their larger spatial extension enables the compensation of the current gain effect by current spreading, which becomes more effective with larger L_{Gate}. This compensation cannot occur for devices built on SOI substrates, since the area of current conduction is largely limited by the thickness of the active silicon layer.

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