A novel sub-20nm Depletion-Mode Double-gate (DMDG) FET

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***Abstract*—We present a novel Depletion-Mode Double-Gate (DMDG) FET. As opposed to the conventional, un-doped body, double-gate MOSFETs, the DMDG device confines the carriers to the center of the device for all applied gate voltages. The device exhibits high mobility due to the carrier confinement in the very low E-field region in the center of the device. Simulations show very high I_{on}/I_{off} ratios (NMOS=2.07mA/25nA, PMOS= 1.02mA/0.98nA), excellent sub-threshold slopes and Fan-Out-Four (FO4) delays under 5.5ps for 15nm gate lengths.**

Keywords-MOSFET; sub-20nm; depletion mode; double gate; body doping; volume inversion; high mobility; carrier confinement;

I. INTRODUCTION

Due to its excellent electrostatic integrity, the double gate (DG) MOSFET is widely considered to be an ideal structure to scale CMOS to sub-20nm dimensions [1], [2]. However, as the channel length is scaled, DG MOSFETs require ultra-thin silicon channels to maintain their electrostatic control over the channel [3], [4]. Theoretical and experimental evidence has shown peak mobility degradation up to a factor of 5 in thin (3-7nm) silicon films [5]. The introduction of High-k dielectrics to reduce the increasing gate leakage in sub-20nm devices further degrades the carrier mobility [6]. The near-equilibrium low-field mobility of inversion carriers is a very key parameter in determining the ON current of a nano-scale MOSFET [7], [8].

In this paper, we propose a novel depletion-mode double-gate (DMDG) FET that allows us to scale CMOS to sub-20nm dimensions by incorporating novel transport principles. The carriers in the DMDG MOSFET, are confined to the center of the silicon body and do not suffer from severe mobility degradation due to the vertical field or due to scattering at the High-k gate dielectric interface. Further, due to the double gate structure, the device exhibits excellent short channel control. This results in enhanced performance of the device in terms of delay and power consumption. A thorough analysis of the DMDG FET is presented through extensive process (TSUPREM), device (MEDICI) and circuit (MEDICI) simulations.

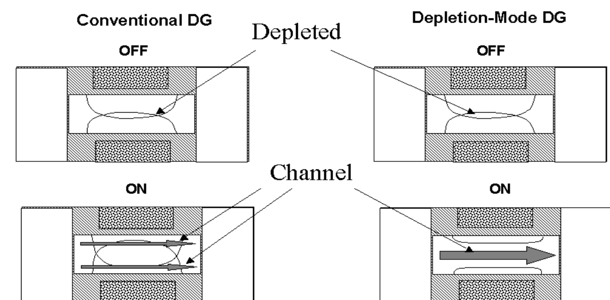

Fig 1: Basic working of the DMDG FET with channel in the center of the body compared to conventional surface channel DG FET

II. DEVICE STRUCTURE AND PHYSICS

A. *Device structure and working*

The basic structure of the DMDG device is described in Fig. 1. As opposed to a conventional structure, the DMDG device consists of a double gate structure where the body is doped with impurities ($N_{a,d}$) of the same type as the source-drain regions. The transistor is fully depleted in the off state by choosing an appropriate gate work function (ϕ_f). Typically, a high work function gate is desired for the NMOS and a low work function gate for the PMOS. Application of a gate voltage decreases the band bending, which reduces the depletion width and creates a channel in the center of the silicon body in the on state. Fig. 2 shows the 2-D electron concentration profile in a typical DMDG NMOSFET, where the channel is formed in the center of the body. In a conventional DG FET, the channels are formed closer to the interface.

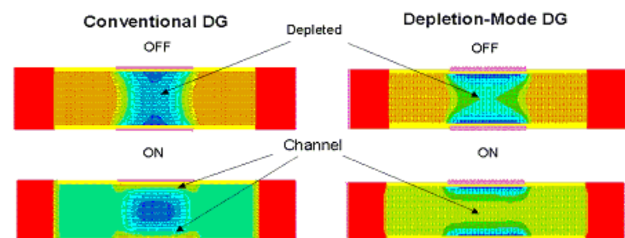

Fig 2: 2-D electron concentration profile of a typical DMDG MOSFET with channel in the center of the body

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B. Higher mobility due to lower vertical E-field scattering

The equation for the saturated drain current in a MOSFET is given by [7]

$$I_{Dsat} = WC_{ox} v_{inj} \left[\frac{1 - r_{sat}}{1 + r_{sat}} \right] (V_{GS} - V_T) \quad (1)$$

where the symbols have their usual definitions. The injection velocity of the carriers at the source is denoted by v_{inj} and r_{sat} is the channel backscattering coefficient in saturation. The backscattering coefficient can be expressed as [7]

$$r_{sat} = \frac{\ell}{\ell + \lambda_0} \quad (2)$$

where λ_0 is the near-equilibrium mean-free-path for backscattering and ℓ is a critical length for backscattering under high bias conditions. Note that λ_0 is directly related to the mobility of the carriers near the source at high gate bias.

In order to increase the saturated drain current in a transistor, it is important to reduce the backscattering coefficient by improving the mobility of the carriers at the source at high gate biases. Fig. 3 shows the vertical electric field along the perpendicular cross section of the device. The symmetry of the double gate structure results in a zero vertical electric field in the center of the channel for all gate biases. Since the DMDG has a peak carrier concentration in the center of the channel where the E-field is zero, the carriers do not suffer significant mobility degradation due to the vertical field. In comparison, a conventional double gate device has two electron peaks close to the interface where the perpendicular electric field is very high. This perpendicular field degrades the electron mobility at high gate biases and consequently reduces the saturated current drive.

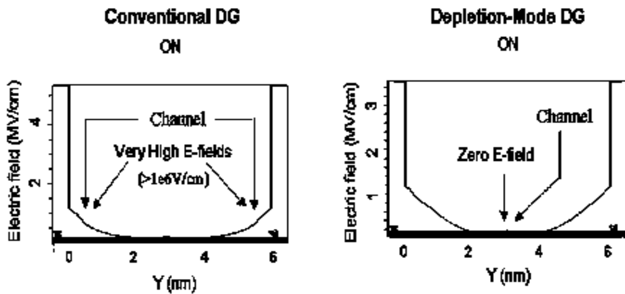

Fig 3: Electric field along a perpendicular cross section of the device showing zero E-field in the middle of DMDG FET where carrier concentration in maximum

Thus, a DMDG MOSFET operates in a very low vertical E-field regime, higher up the universal mobility curve. The carriers are also further away from the interface than a conventional MOSFET and do not suffer from significant interface scattering. However, since the body is doped, the carriers do suffer some mobility degradation due to ionized impurity scattering. Decoupling the channel from the interface in the DMDG device also allows for easier integration with High-k dielectrics.

C. Threshold voltage

The threshold voltage of the DMDG device is set by the gate work function (ϕ_f) and the total charge that can be depleted by the gate (Q) in order to turn the device off. This charge (Q) is proportional to the product of the channel doping ($N_{a,d}$) and the silicon channel thickness (t_{si}). Fig. 4 and Fig. 5 show the dependence of the device threshold voltage (V_t) on $N_{a,d}$ and ϕ_f.

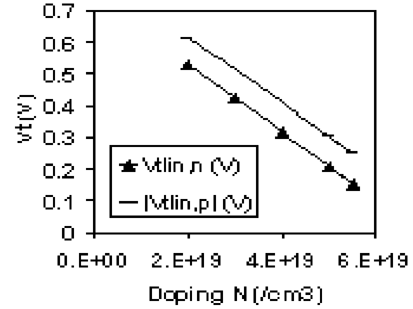

Fig 4: Linear Threshold voltage (Vt,lin) (NMOS/PMOS) as a function of channel doping (Na,d)

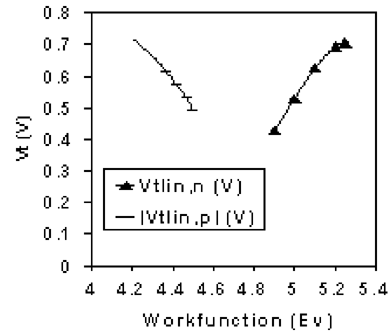

Fig 5: Linear Vt (NMOS/PMOS) as a function of gate workfunction (ϕf)

In the next section, we present the device performance in terms of short channel effects, I_{on}/I_{off} characteristics and Fan-Out-Four (FO4) power-delays.

III. SIMULATION RESULTS

A. Device characteristics

To obtain the device characteristics, the nominal device was chosen to have a 12.5nm channel length with a 5nm body thickness. Fig. 6 and Fig. 7 show the typical I_d-V_g characteristics of a DMDG NMOS and PMOS respectively. The higher mobility, due to lower vertical E-field scattering, results in high drain currents. The I_{on}/I_{off} ratios obtained for these devices are very high (NMOS=2.07mA/25nA and PMOS=1.02mA/0.98A). Since the carriers in a DMDG FET are concentrated in the center of the channel and not at the surface, the capacitance is slightly lower than a conventional DG ($C_{gs} \approx$ 0.3 femtoFarads/µm), as shown in Fig. 8 and Fig. 9. All these factors lead to better circuit performance, as seen from the circuit simulations presented in section C.

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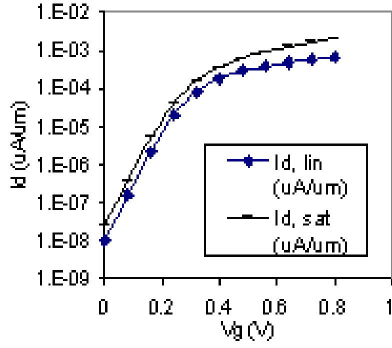

Fig 6: NMOS characteristics for device with L=12.5nm, tsi=5nm. Ion/Ioff = 2.07mA/25nA

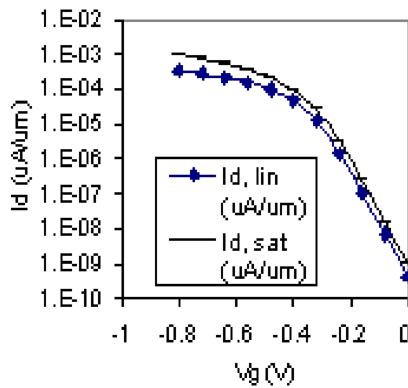

Fig 7: PMOS characteristics for device with L=12.5nm, tsi=5nm. Ion/Ioff = 1.02mA/0.98nA

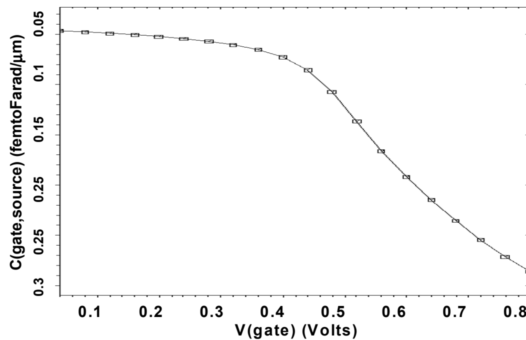

Fig 8: Capacitance of NMOS with gate oxide (tgox) = 5A, tsi =5nm (< 0.30 femtoFarad/µm)

B. *Short- channel effects and silicon thickness (t_{si}) variation*

The DMDG device exhibits excellent short channel effects due to the superior electrostatics of the double gate structure. Fig. 10 and Fig. 11 show very small threshold voltage roll off (ΔV_t<0.04V) and nearly ideal sub-threshold slope (s<70mV/decade) over a 100% variation in channel length respectively.

Decreasing the silicon body thickness in DG FETs increases the threshold voltage [5]. In the DMDG FET, decreasing the body thickness (t_{si}) also reduces the charge under the gate (Q) and hence increases the threshold voltage (V_t) of the device. Fig. 12 shows a low change in the V_t with variation in t_{si}.

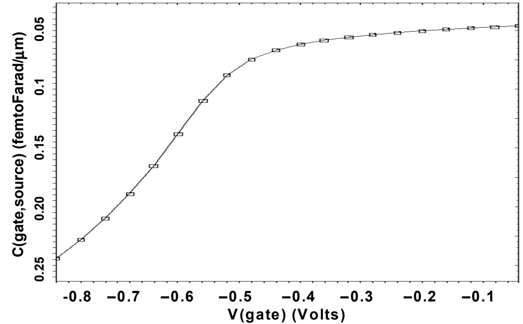

Fig 9: Capacitance of PMOS with gate oxide (tgox) = 5A, tsi =5nm (<0.25 femtoFarad/µm)

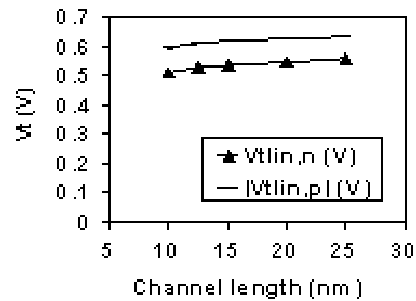

Fig 10: Linear Vt (NMOS/PMOS) variation with channel length (L)

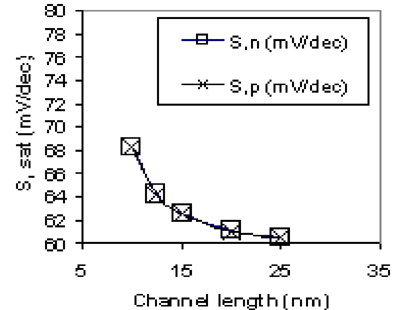

Fig 11: Sub-threshold slope (s) (NMOS/PMOS) variation with channel length (L)

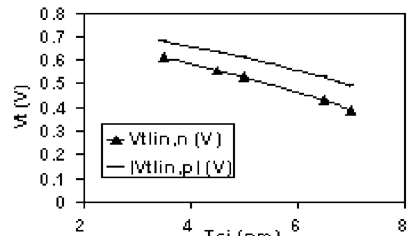

Fig 12: Linear Vt (NMOS/PMOS) variation with silicon thickness (tsi)

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C. *Fan-Out-Four (FO4) Power-delay*

Fan-Out-Four (FO4) power-delays are universally accepted as excellent metrics of true circuit performance of a device. In order, to reflect the performance of a fabricated device, the DMDG devices were optimized around a 15nm gate length, subject to constraints imposed by process variations during the fabrication of a device. The fabrication process steps were simulated using TSUREM and the device was simulated using MEDICI. Fig. 13 shows the FO4 delays obtained for such a device. The device exhibits very fast rise times (5.5ps) and fall times (4.6ps). The integrated current consumed, during switching, by a three-stage FO4 inverter chain is shown in Fig. 14. The power consumed (460µW) by the switching activity is also found to be very low.

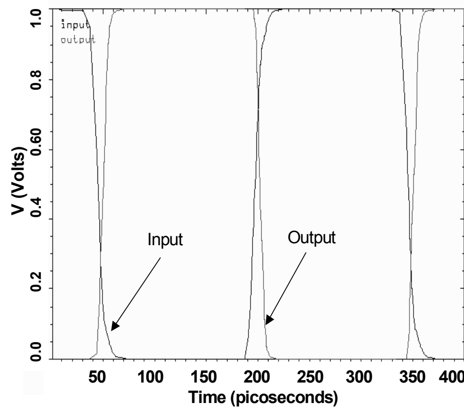

Fig 13: Fan-Out-Four (FO4) delay of inverter. (Rise-time=5.5ps, Fall time=4.6ps)

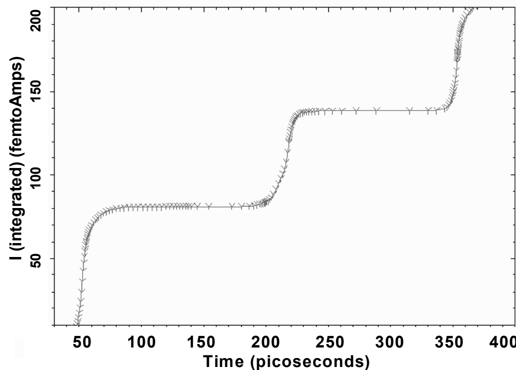

Fig 14: Integrated current consumption by 3-stage FO4 inverters at 1V

IV. Conclusions

In summary, we have presented a novel Depletion-Mode Double-Gate (DMDG) MOSFET, which shows enhanced performance by exploiting new transport ideas. The carriers in the DMDG FET are confined to the center of the silicon body and do not suffer from mobility degradation due to the vertical field because of the zero vertical E-field in the center of a double gate device. Since, the carriers are pushed away from the interface, they are not significantly affected by scattering at the semiconductor-insulator interface. This allows for easier integration with High-k dielectric materials. However, due to the doped body, the carriers suffer some mobility degradation, primarily due to ionized impurity scattering. Process, device and circuit simulations verify that the DMDG FET exhibits excellent short channel control, low threshold voltage variation with the body thickness and high I_{on}/I_{off} ratios. The device has a very good circuit performance in terms of FO4 power-delays and shows great potential in scaling devices down to sub-20nm dimensions.

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