A New Comprehensive SRAM Soft-Error Simulation Based on 3D Device Simulation Incorporating Neutron Nuclear Reactions

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***Abstract*— A new SRAM soft-error simulation tool has been developed and its accuracy was evaluated through both acceleration tests for α-particles and energetic neutron beam irradiations. This simulation was able to reproduce the measurement data for the soft-error rate of a 0.15-μm SRAM (test-chip) within a factor of two, including the power supply voltage dependency. The simulation system consists of several sub-parts, and features a new data-set for neutron/silicon-atom nuclear reactions and the use of a three-dimensional device simulator for calculating precise charge collection amounts. This accurate simulation can be used for quantitative evaluation of competing effects by means of reduced critical charges and cell-area reduction, and have applications in developing future SRAM technology.**

I. INTRODUCTION

CMOS-SRAM and logic circuit elements have been facing serious reliability issues because of soft errors under standard environments[1]. The dominant sources of the soft errors have been shown to be α-particle, ^{10}B in BPSG and cosmic-neutrons[2]. Several studies have already been carried out on current SRAM technology[3] and emerging SRAM technology[4], using not only experimental evaluation but also simulation attempts including high-energy neutron effects[5]. However, the reliability of the simulation approach itself is rarely discussed, and evaluations of technology-dependent soft-errors still rely on long-term expensive experimental observations[1][6].

This paper describes a new comprehensive modeling and simulation approach capable of providing precise evaluations in comparison to the use of both α-particles and energetic neutron beam irradiation tests. The new simulation also has capability beyond actual experimental evaluations. For example, it can be used to clarify the coupling (competing) of several effects, i.e. the effect of individual contributions such as different supply-voltage effects, different critical charge effects, or reduced cell-size effects, in observing the net soft-error-rate (SER). Therefore it can also be applied in analyzing SER sensitivity of the high-reliable memory systems.

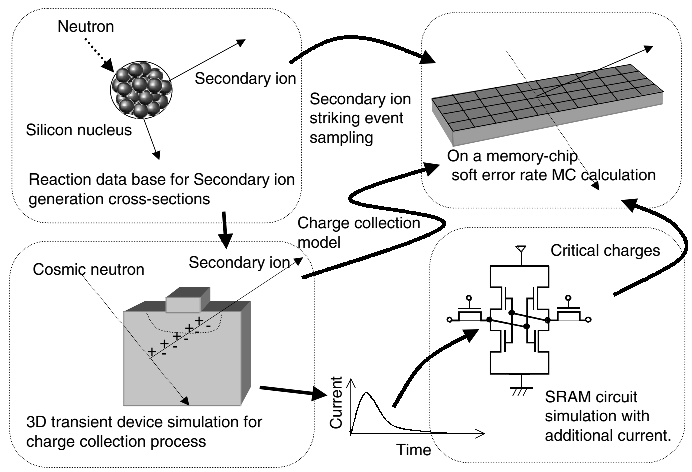


Fig. 1. SRAM soft error rate (SER) simulation system consisting of (i) nuclear-reaction database, (ii) 3D transient device simulator, (iii) circuit simulator (SPICE) and (iv) Monte Carlo SER calculation program.

II. SIMULATION METHOD

This simulation system consists of four-parts: (1) recent wide-ranging and well-established nuclear reaction data for energetic neutron and silicon nuclei, (2) 3D transient device simulation for determining dynamic charge collection amounts, (3) SRAM circuit simulation for determining the critical charge (Q_c) for error criteria, and (4) a SRAM cell-layout dependent multi-bit error count calculation component based on Monte-Carlo (MC) procedures for sampling primary/secondary ion striking events. Figure 1 illustrates our simulation scheme and the correlation of individual simulators. For the MC component, more than 100 million sampling simulation of primary/secondary particle striking events were performed on the periodic unit-cell structures of SRAM cell layouts.

Our neutron/silicon nuclear reaction data-set covers a typical cosmic-neutron energy range on earth: JENDL-3.3 for 1-20MeV [9], LA150 for 20-150MeV [10], and QMD (Quantum

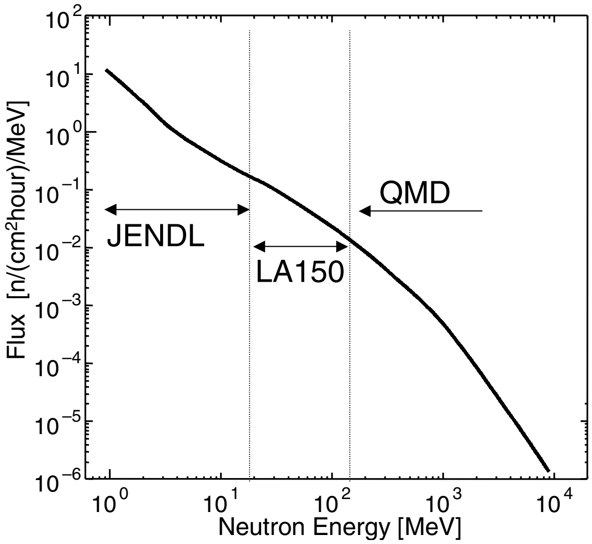


Fig. 2. Our neutron/silicon nuclear reaction data-set covering a typical cosmic-neutron energy range on earth, JENDL-3.3 for 1-20MeV [9], LA150 for 20-150MeV [10], and QMD (Quantum Molecular Dynamics) calculations for >150MeV[11]. Neutron energy flux data shown in this diagram, are taken from [14].

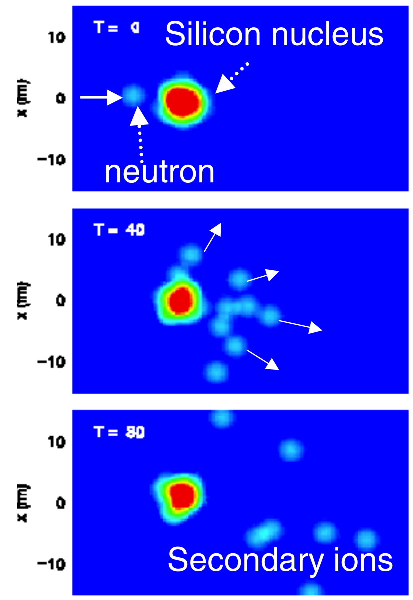


Fig. 3. Examples of QMD calculation results. About one million QMD calculations were performed combined with SDM (Statistical Decay Model) per a sampled incident neutron energy [12].

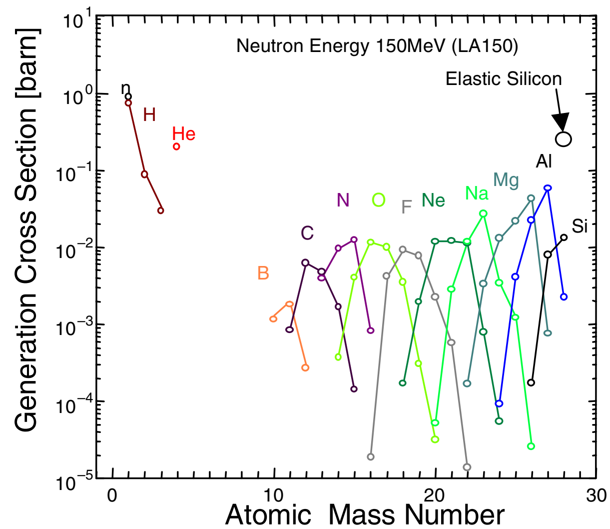


Fig. 4. Secondary ion generation cross-sections for Neutron/Silicon-nuclei reaction.

Molecular Dynamics) for $>$ 150MeV[11] (Figs.2-3). Figure 4 shows the generation probability of typical secondary ions produced by nuclear reaction between an energetic neutron and a silicon nucleus. About one million QMD calculations were performed combined with the SDM (Statistical Decay Model) per an sampled incident energy [12].

For given α-particle or neutron flux, the MC program component calculates numerous samples of ion striking events, then converts all the collection charge values to the single-event-upset rate using the Qc criteria. A 3D device simulator[13] is used not only for obtaining typical spike-current wave-forms for the circuit-simulation (SPICE) but also for obtaining precise charge collection efficiency maps in the 3D unit-cell volume of the memory cells (Fig.5). The charge collection events are calculated on the basis of the line charge along an ion trajectory that penetrates the unit-cells, which often causes funneling effects. A typical current-pulse wave form, calculated under the α-particle normal incident condition, is shown in Figure 5.

The primary/secondary ion striking events are pre-calculated according to the structure of the device cell with several different incident position and angles[7]. The trajectories of the ions in the SRAM cells are calculated on the basis of the TRIM code[8].

Some particular angle incidents show a collective charge gain due to funneling and bipolar-action gain effects. Figure 6 shows examples of the charge collection efficiency map for cases of horizontal ion penetration, calculated using the 3D transient-device simulator, with consideration given to the actual doping structure of the transistors. Collected charge gain effects can be seen for the collection charge amount at the cell nodes ($Q_{col} > Q_{gen}$). Such specific bipolar-action gain effects can be efficiently incorporated in this simulation scheme. Thus, our simulation does not require the fitting of parameters, such as an effective funneling length or a sensitive volume for charge collection which are mostly for reproducing previous experimental data but not for predicting new device reliability. The purpose of our simulation is to evaluate soft-error immunity and provide process/device design feedback.

III. Results and Discussions

Two types of acceleration tests were performed on 0.15-μm SRAM test-chips that included single-port and dual-port configurations. One test used ^{241}Am for the α-particle source,

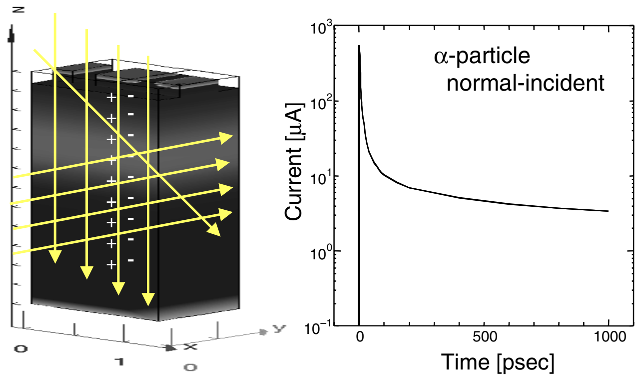


Fig. 5. 3D device simulations are performed to obtain current pulse wave forms and to construct 3D charge collection efficiency maps depending on charged particle incident positions and angles. The charge collection events are calculated based on the line charge along the ion trajectory penetrated into the unit-cells which often causes funneling effects. A typical current pulse wave form, calculated under the α-particle normal incident condition, is also shown.

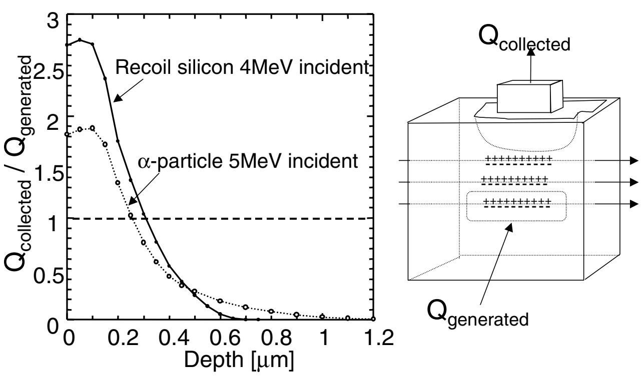


Fig. 6. Examples of the charge collection efficiency map for cases of horizontal ion penetration, calculated by a 3D transient device simulator that considered the actual doping structure of the transistors. Gain effects ($Q_{col} > Q_{gen}$) can be seen for the collection charge amount at the cell nodes.

and the other was a high-energy neutron beam irradiation test carried out at the Los Alamos National Laboratory. The simulations were performed under both a given α-particle flux and a neutron energy flux. 2D process/device TCAD simulations were also performed to verify the precise doping structure required for 3D device simulation. Circuit simulations gave us different Qc for single-port or dual-port cells. The simulation results reproduced experimental data within a factor of $0.5\times$ for α-particle acceleration tests, and within a factor of $2\times$ for neutron-beam irradiation tests. The dependency of the power supply voltages could be also reproduced by this simulation.

The single-power-law seems to hold sufficiently for the α-particle irradiation test as shown in Figure 7(b), but not for the neutron irradiation test as shown in Figure 8. This is because more than two groups of secondary ions contribute to the sub-linear dependency of the supply voltages on the SER in the case of high-energy neutron irradiation tests. Our simulation can clarify the contribution of light ions (H, He, Li, ...) under

(a)

(b)

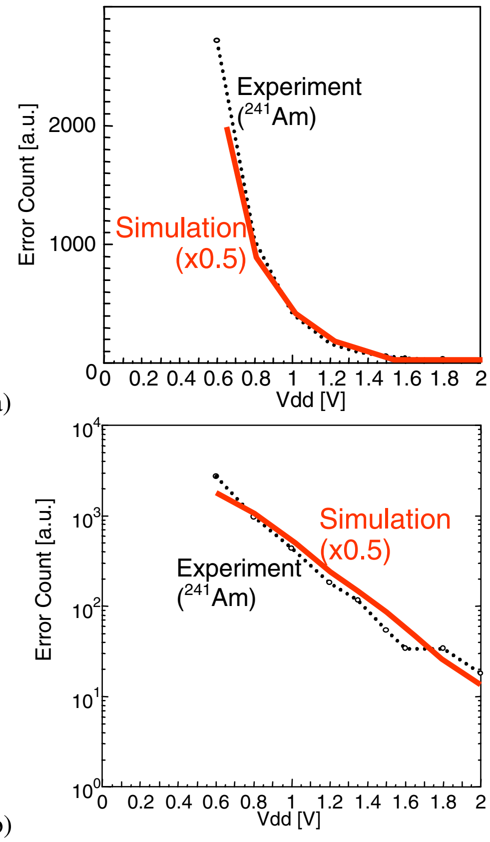


Fig. 7. Comparison between simulation and measurement for ^{241}Am acceleration test. (a) Linear-scale representation, (b) log-scale representation.

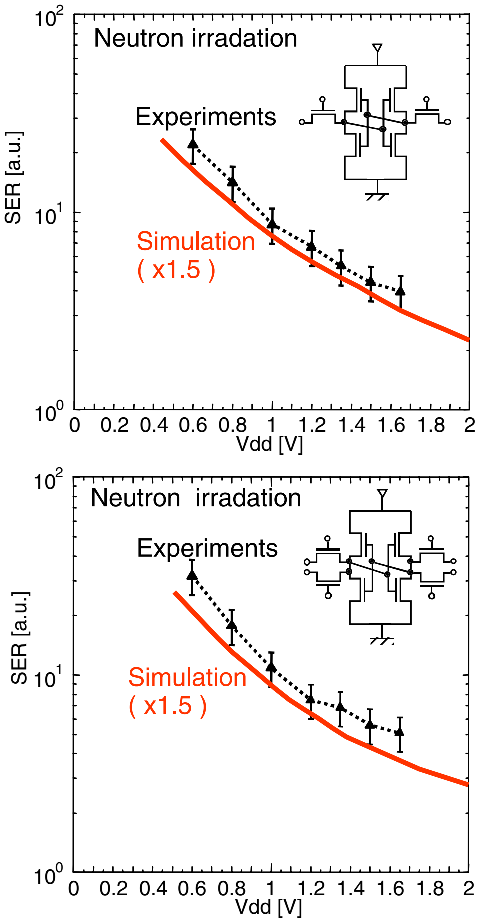
low supply voltage conditions in addition to that of the heavy ones (..., Mg, Al, Si).

The simulation results also show good agreement between different SRAM (test-chip) cell configurations (single- or dual-port). The Q_c and source/drain areas of the single-port cells are about half the size of those of the dual-port cells. A simulation assuming an identical structure except for reducing Q_c values showed enhanced-collection-charge events, and thus increase SER. In contrast, simulation in which the source/drain area was artificially reduced while the Q_c was kept constant, gave smaller SER values.

As shown in Figure 9, our quantitative simulation and actual experimental verification showed that both effects are competing and that the cell-area reduction effect is slightly superior at giving smaller net SER values for SRAM chips with reduced Q_c and cell-areas. This finding can be extended to situations relating to advanced future-generation SRAM technology (i.e. reducing both Q_c and cell-area).

IV. Conclusion

A new SRAM soft-error simulator was developed and its accuracy was verified through both α-particle and high-energy neutron acceleration tests for the latest CMOS-SRAM technology. This simulator is not only able to reproduce experimental data but also to provide in-depth analysis of



(a)

(b)

Fig. 8. Comparison between simulation results and measurement data for high-energy neutron beam acceleration tests. (a) Single-port cells, (b) dual-port cells.

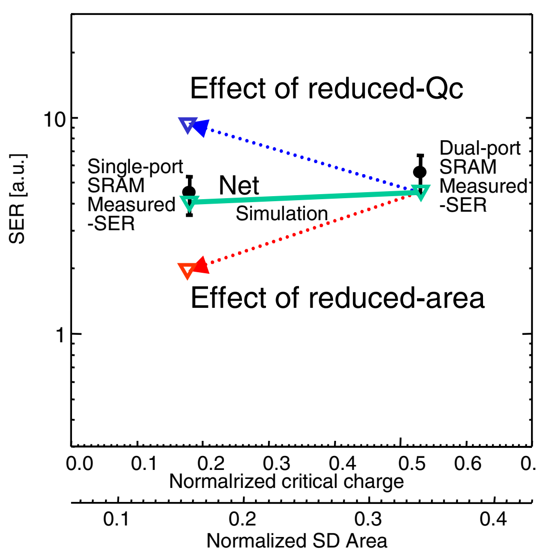


Fig. 9. Comparison between simulation (lines) and measurement (plots with error-bars) for SRAM (test-chip) cells with different configurations: single-port and dual-port. The single-port cells have about half the source/drain area and half the Q_c values, of the dual-port cells.

coupling (competing) effects. It therefore has applications in analyzing future technology prospects.

Acknowledgment

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