# Simulation of the Circuit Performance Impact of Lithography in Nanoscale Semiconductor Manufacturing

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*Abstract*— **With nanoscale semiconductor technology, circuit performance is increasingly influenced by details of the manufacturing process. An increasing number of manufacturing features, which are not included in standard design tools, affect both circuit performance and yield. One source of circuit performance degradation is lithography imperfections. Therefore, we need to simulate how lithography imperfections impact circuit performance. Such imperfections include the proximity effect, lens aberrations, and flare. These imperfections in lithography impact circuit timing. This paper introduces a method to incorporate the proximity effect, lens aberrations, and flare in timing simulation. Our method involves expanding and revising the cell library by considering optical effects. ISCAS benchmark circuits are used to evaluate the circuit performance impact of each optical effect.**

***Keywords-DFM; nano-technology; lithography***

## I. INTRODUCTION

Scaling of semiconductor processing has enabled the production of higher performance products at lower cost. However, implementing products on advanced technologies is increasingly challenging because deep submicron technologies are associated with increasing numbers of unsimulated features and design-process interdependencies. One important source of a discrepancy between design and manufacturing relates to imperfections in lithography, especially associated with printing the transistor gate and controlling its critical dimension (CD). Until recently, worst case analysis was an adequate tool to model gate CD variability and to predict the distribution of chip speeds. Today, a significant component of CD variability is variation within the chip, which systematically degrades circuit speed [1].

The current paper is not the first attempt to include optical effects in the simulation of circuit speed. In [2], Chen proposed a method to determine circuit speed in the presence of the proximity effect. The approach involved extracting CD corrections based on the circuit's layout and the neighboring features of each gate, which were then translated into modified channel lengths of transistors in HSPICE [3] files for the critical paths. HSPICE was then used to determine the critical path delays. In [1], Orshansky improved the previous approach by considering both the proximity effect and lens aberrations and by replacing HSPICE simulations with static timing analysis. However, only the simulation of small blocks was considered. Further improvements are required to handle analysis of complete chips.

In this work, we simulated the timing of ISCAS circuits with gate CDs affected by the proximity effect, lens aberrations, and flare, in order to improve our understanding of the relationship between imperfections in gate layer lithography and circuit speed. The gate CD is a function of its neighborhood [2],[4], because of the proximity effect. Lens aberrations result in CD variations as a function of position within the chip [5]. Finally, flare is caused by scattering [6], which causes the gate CD to be a function of mask density.

This paper is organized as follows. Section II describes our simulation flow. In Section III, the impact of each optical lithography effect on circuit performance is analyzed. Section IV concludes the paper.

## II. SIMULATION FLOW

Static timing simulation sums up the delay of cells in critical paths, where the delays are a function of the rise time of input signals and the loading of capacitance [7]. This information is captured in cell delay tables. Imperfections in lithography modify the gate CDs based on neighboring gates in the layout (proximity effect), the placement of the cell in the layout (lens aberrations), and the density of features on the mask (flare). Since the gate CDs change as a function of the location and the neighborhood, the cell delay tables also change. Consequently, taking into account lithography in static timing analysis involves revising cell delay tables to account for cell neighborhood and location.

Cell names are relabeled, indicating cell location and the poly density of the neighborhood. This new cell name replaces the original name in the HDL file. Thus several versions of every cell are generated, each corresponding to different layout data and enlarging the cell library. Transistors of the cell HSPICE file are tagged, indicating neighborhood information, as was done in [1] and [2]. Data on the proximity effect, lens aberrations, and flare can now be used to modify transistor CDs

for every transistor in the chip layout. The next step is to generate revised cell delay tables for all cells in the layout. This is done using *Avant! Hspice* [3]. Then, conventional static timing analysis is performed by *Synopsys Design Analyzer* [8]. Our simulation flow is shown in Figure 1.

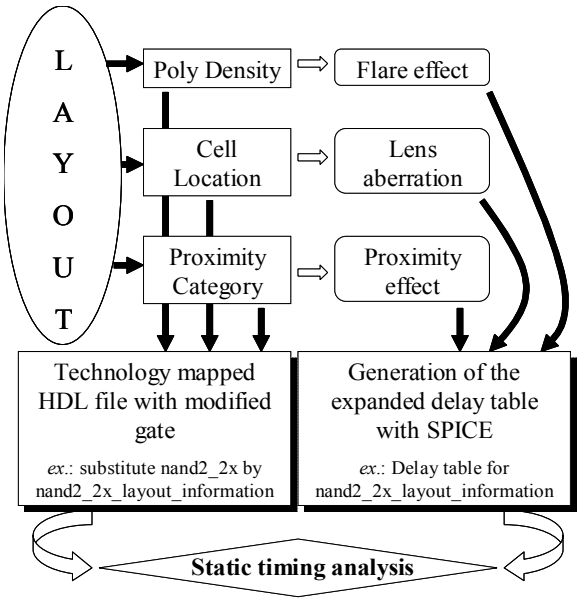



Fig. 1. Flow chart.

### A. The Proximity Effect

The gate CD depends on its neighborhood due to the proximity effect. We account for the neighborhood by determining the distance to the nearest poly geometry on the left and on the right of each transistor gate, as in [2]. Each transistor, therefore, has two labels, the distance to the nearest poly geometry on the left and the distance to the nearest poly geometry on the right. These two labels combine to determine the category of each gate. Our script has been implemented with *Mentor Graphics Calibre* [9]. In our examples, the distances to the left and to the right are labeled as n1 to n5, where n1 is the minimum poly spacing (Smin). The largest distance is n5, which corresponds to all distances greater than 2.5Smin. The distance categories are illustrated in Figure 2.

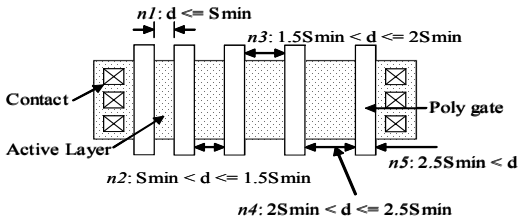



Fig. 2. Distance Categories.

The proximity effect between cells was ignored in [2]. However, as the technology is advancing, it is no longer appropriate to ignore inter-cell effects. Therefore, we have included the inter-cell proximity effect by adding a label to the cell name.

Finally, the Coma effect not only depends on the distance to the neighboring cells, but also requires that we distinguish between features to the left and features to the right. If the cell is flipped during the placement and routing step, the labels of all gates need to be reversed, i.e. distances to the left become distances to the right, and vise versa. We indicate this by adding a label to the cell name signifying if the cell has been flipped (f) or not (n).

### B. Lens Aberrations

Accounting for lens aberrations involves determining the location of the gate in the layout. The placement and routing tool (in our case, *Cadence Silicon Ensemble* [10]) gives us information about the cell location. The layout is partitioned by a grid. We look up the location of each cell with respect to the grid and attach a label to the cell name indicating its location. Because lens aberrations and the proximity effect interact, gate CDs are a function of their location *and* neighborhood.

### C. Flare

Because of flare, the gate CD depends on the mask density. Therefore, the gate CD is determined by computing the percent chrome of the mask in the neighborhood of the gate. The range of the neighborhood is currently not well understood, and therefore, in our tool, it is a user input. First, the poly area of each cell is calculated using *Mentor Graphics Calibre* and our Perl Script. Second, the cell list in each sector is obtained from the report of the placement tool. Third, we sum up the poly area of the cells in each sector and calculate the poly density. Fourth, the poly density of each sector is recorded in the poly density file and the cell name is tagged by the sector as was done for lens aberrations. The procedure is shown in Figure 3.

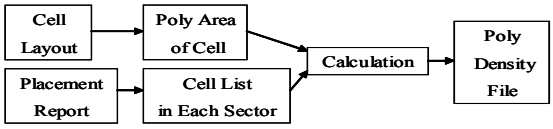



Fig. 3. Procedure for Poly Density Calculation.

### D. Genration of the expanded table for Cell Characterization

We can obtain CD maps for each category and location and CD variation data by flare effect from test structures used to characterize the semiconductor process line. We can also obtain a list of all cells and their locations in the layout from the placement tool. The gate CDs can be updated in the HSPICE file using the modified cell name, the tagged HSPICE file, and the experimental CD data.

The algorithm selects the appropriate CD from the experimental CD maps and updates the channel lengths in the HSPICE file based on the proximity category and the layout information. Then, the flare experimental data gives us the scattering influenced CD as a function of poly density. The channel lengths in the HSPICE file are updated accordingly. The algorithm is summarized in Figure 4.

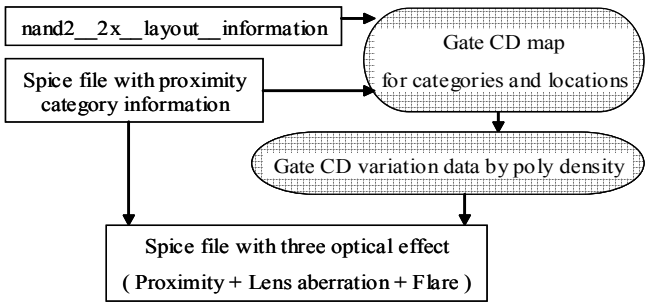



Fig. 4. Algorithm for obtaining the correct CD from the modified cell name, the tagged HSPICE file, and the experimental data.

### *E. Computational Efficiency*

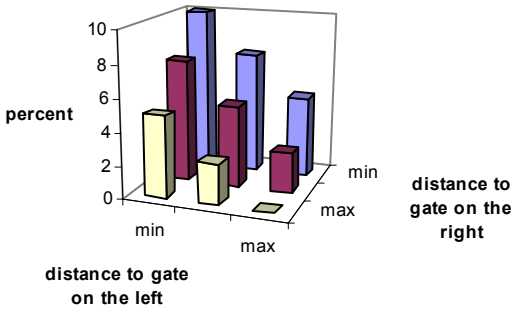
A key challenge of this work is the management of the data and the computational complexity. Typical designs involve 200-300 cells. Accounting for the impact of lithography on CD values requires the discretization of CD values as a function of location within the reticle and the local neighborhood. The level of discretization determines the number of versions of each of the 200-300 cells. For timing analysis, each version has to be characterized using HSPICE with modified CDs. In order to avoid the characterization of thousands of cells, we have organized the computation so that we determine the cells in the likely critical paths, prior to characterization.

In order to demonstrate our timing analysis method, two ISCAS benchmark circuits (c7552, c6288) [11] have been implemented with a standard cell library with 132 cells and partitioned into 25 areas. We potentially require characterization of 132 x 25 cells. The computational cost of static timing analysis is dominated by the cost of generating the delay tables which is proportional to the number of cells in the cell library. Hence, incorporating optical effects increases the computational cost by over an order of magnitude. However, by analyzing the likely critical paths, we can reduce the number of cells requiring characterization to 20 for each of the example circuits.

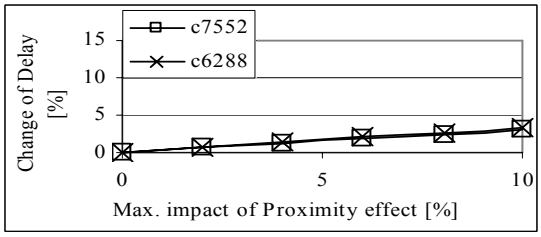
## III. IMPACT OF EACH OPTICAL EFFECT

We have evaluated the sensitivity of delay to lithography effects for two ISCAS benchmark circuits (c7552, c6288) [11], implemented with a standard cell library with 132 cells and partitioned into 25 areas. For each of our examples, we have considered only one factor at a time. This study allows us to determine which lithography components require the most effort for correction.

Let's first consider the proximity effect. We have considered the situation where the gate CD is a function of distance to the nearest neighbors, with no Coma effect [4]. The proximity effect causes some CDs to be larger than desired, while others are minimally impacted, as shown in Figure 5(a). The minimum CD is normally the minimum manufacturable transistor, as it is also the most leaky transistor. As can be seen from Figure 5(b), the sensitivity to delay reflects the average impact on cells in the critical paths. We can therefore conclude that minimizing the range of variability will improve circuit speed, since the average CD in the critical path will become closer to the minimum CD. In other words, as the maximum impact of the proximity effect increases to 10%, the average impact increases to 5%, and the delay increases by almost 5%.

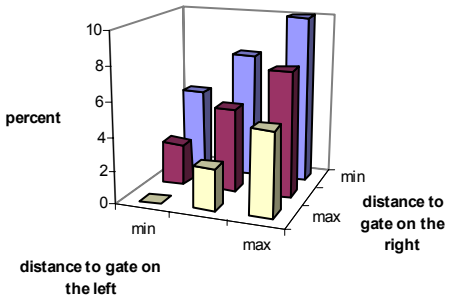



(a) CD variation of each of the gate categories

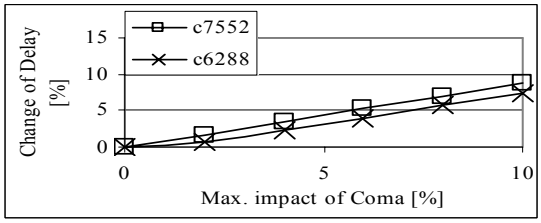



(b) Delay variation

Fig. 5. Delay sensitivity to the proximity effect.




(a) CD variation of each of the gate categories




(b) Delay variation

Fig. 6. Delay sensitivity to Coma.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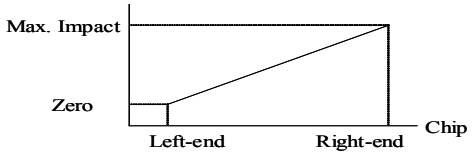
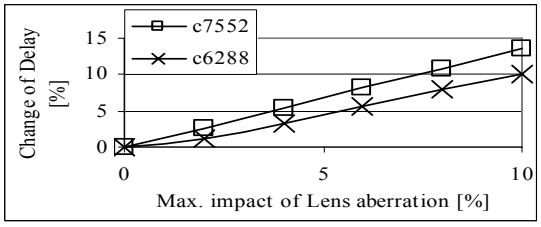
Second, we considered the situation where the gate CD is a function of Coma only. Figure 6(a) shows us the asymmetrical impact of Coma. Figure 6(b) shows the simulation result. As with the proximity effect, as the maximum impact of Coma reaches 10%, the average impact approaches 5%, and the delay increases by 5-10%.

Next we considered the impact of lens aberrations and assumed that the gate CD varied by up to 10%, from one side of the chip to the other, as shown in Figure 7(a). All CDs of a cell change equally. When the impact is 10%, the delay change is over 10% as shown in Figure 7(b). This indicates that critical paths are not distributed throughout the chip, and as a result, delay is a function of the worst case increase in CD for lens aberrations.

Finally, we considered the impact of flare. We have assumed that a gate is influenced by a neighborhood with a radius of 75um. The cells of some of the critical paths appear to have an above average poly density. The simulation result is shown in Figure 8. Again, delay is a function of the worst case situation, rather than the average CD (proximity effect and Coma).




(a) CD variation due to lens aberrations



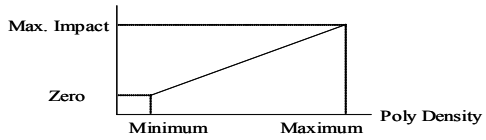

(b) Delay variation

Fig. 7. Delay sensitivity to lens aberrations.

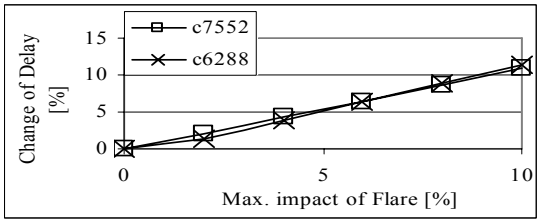
## IV. CONCLUSIONS

We have developed a tool to simulate circuit delay while taking into consideration the proximity effect, lens aberrations, and flare. The cell name is labeled by information needed to account for lens aberrations and flare. Neighborhood information relating to the proximity effect on individual transistors is reflected in HSPICE files of cells by tags on the transistor names. Optical dependent delay tables are generated for each cell using these HSPICE files. As a result, the cell library for timing analysis is expanded and revised to account for optical effects. The challenge of our methodology has been the explosion of the number of cells in the cell library. This challenge is overcome by considering only cells on the critical paths (prior to the introduction of optical effects) and could be further improved by focusing on the operating points in the delay tables.

We investigated the impact on circuit delay of various optical effects. Our simulations involved critical paths in ISCAS circuits. The results tell us that delay is affected by the average CD from the proximity effect and Coma. However, delay is a function of the worst case CD from lens aberrations and flare. These results guide us towards prioritizing the use of techniques to correct optical effects, and can help us reduce manufacturing risk associated with newly emerging imperfections in nanoscale semiconductor manufacturing.




(a) CD variation due to flare effect




(b) Delay variation

Fig. 8. Delay sensitivity to flare.

## ACKNOWLEDGMENT

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