Compact Modeling of Flash Memory Cells Including Substrate-Bias-Dependent Hot-Electron Gate Current

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***Abstract*— We propose a compact model for flash memory cells that is suitable for SPICE simulation. The model includes a hot-electron gate current model that considers not only Channel Hot Electron (CHE) injection but also CHannel Initiated Secondary ELectron (CHISEL) injection to express properly substrate bias dependence. Simulation results of both programming and erasing characteristics for 130nm-technology flash memory cells indicate that our model is useful in designing and optimizing circuit for flash memories.**

I. Introduction

Flash memories are indispensable for mobile equipments because of their nonvolatility. A growing need to process more complicated task on these equipments requires flash memories to have larger capacity and lower power consumption, which leads to finer wafer process and more complex circuit design. Therefore, circuit simulation becomes very important in circuit design and optimization for flash memories.

Programming efficiency, which is defined as a ratio of gate current to programming current, is one of the most important factor for flash memories to determine power consumption and programming speed. The programming efficiency of flash memory cells which utilize hot-electron injection to program is enhanced by applying substrate bias[1][2][3][4]. Mechanisms of the enhancement by substrate bias have been investigated from device physics perspective of view by measurements[5][6][7] and simulations[8][9]. From circuit level perspective of view, some work has been done to construct a compact model for the substrate-bias-dependent gate current[10], but a closed-form model has not been proposed yet. In this work, we propose a SPICE friendly compact model for gate current and show simulation results of the programming/erasing characteristics of a flash memory cell.

II. Modeling

A flash memory cell has a floating gate (FG) between a control gate (CG) and a channel of an MOSFET. Electrons are injected into the floating gate in program mode, whereas they are released in erase mode. These operations are expressed by an equivalent circuit of an MOSFET and a capacitor with two current sources as shown in Fig. 1[11][12]. Model parameters for $I_{\rm ds}$ and $I_{\rm sub}$ of the MOSFET are extracted to fit measurement data of a dummy cell, in which bias can be directly applied to the floating gate. Capacitance between FG and CG is extracted to fit a measured coupling coefficient $r_{\rm cp} \equiv \Delta V_{\rm FG}/\Delta V_{\rm CG}$. Gate currents, $I_{\rm gd}$ and $I_{\rm gb}$, are described below.

A. Hot-Electron Injection

A gate current in program mode is expressed as

$$I_{\rm gd} = I_{\rm CHE} + I_{\rm CHISEL}, \tag{1}$$

where $I_{\rm CHE}$ and $I_{\rm CHISEL}$ are injection currents by Channel Hot Electron (CHE) and CHannel Initiated Secondary ELectron (CHISEL), respectively. These components, which are shown in Fig. 2, will be modeled using a lucky-electron model[13][14]. Based on the lucky-electron model, the probability of an electron acquiring the sufficient kinetic energy from the electric field, E, and retaining the appropriate momentum after elastic collision is expressed as[14] $p_{\rm inj}(E) = (E\lambda/4\Phi_{\rm b})\exp(-\Phi_{\rm b}/E\lambda)$, where λ is the inelastic scattering mean-free-path of the hot electron. The effective barrier height $\Phi_{\rm b}$ including the barrier lowering effects due to the image field and the tunneling is expressed as[14] $\Phi_{\rm b}(E_{\rm ox}) = \Phi_{\rm b0} - \Phi_{\rm b1}\sqrt{E_{\rm ox}} - \Phi_{\rm b2}E_{\rm ox}^{2/3}$ when $E_{\rm ox} > 0$ and $\Phi_{\rm b}(E_{\rm ox}) = \Phi_{\rm b0}$ when $E_{\rm ox} < 0$, where $E_{\rm ox} \equiv (V_{\rm gs} - V(x) - \phi_{\rm wf})/t_{\rm ox}$ is the electric field in the gate dielectric film and $\phi_{\rm wf}$ is the work-function difference between silicon substrate and gate electrode.

The CHE component comes from energetic channel electrons which are accelerated by channel electric field. The channel potential, $V(x)$, in the velocity saturation region is

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proportional to $\exp(x/\ell_c)$, and the channel electric field E_x is expressed as $E_x = (V(x) - V_{dsat})/\ell_c$, where ℓ_c is the characteristic length which is determined by the thichness of the gate dielectric film and the drain-substrate junction depth[15]. An electron which surmounts the potential barrier is swept into the gate electrode in the region where $E_{ox} > 0$, whereas it may be pushed back to the channel in the region where $E_{ox} < 0$[16]. The injection, however, occurs in the latter region because some electrons have momentum which is large enough to reach the gate electrode against the electric field in the gate dielectric film. As shown in Fig. 3, the channel potential is $V_{gs} + \phi_{wf}$ at the point where $E_{ox} = 0$, and it increases monotonically toward V_{ds} along the channel direction. The channel potential at the critical point, $x = x_m$, beyond which the electron is pushed back, is between $V_{gs}+\phi_{wf}$ and V_{ds}. We express the channel potential at the point as $V(x_m) = r_d(V_{gs} + \phi_{wf}) + (1 - r_d)V_{ds}$ using the fitting parameter $r_d \leq 1$. The electric field at the point x_m is, therefore, $E_m = (r_d(V_{gs} + \phi_{wf}) + (1 - r_d)V_{ds} - V_{dsat})/\ell_c$ when $V_{ds} > V_{gs} + \phi_{wf}$ and $E_m = (V_{ds} - V_{dsat})/\ell_c$ when $V_{ds} < V_{gs}+\phi_{wf}$. Integrating the product of the channel current I_{ds} and the injection probability p_{inj} from $x = 0$ to $x = x_m$ along the channel, the gate current by CHE injection is

$$I_{CHE} = A_d I_{ds} \left(\frac{\lambda E_m}{\Phi_{bd}}\right)^2 \exp\left(-\frac{\Phi_{bd}}{\lambda E_m}\right), \qquad (2)$$

where $\Phi_{bd} = \Phi_b(E_{ox}(x_m))$ and A_d is a fitting parameter.

The CHISEL component comes from energetic electrons which are generated by hole impact ionization in the substrate and accelerated by vertical electric field. The generated current by hole impact ionization in the substrate, I_{subgen}, is calculated by integrating hole impact ionization coefficient $\alpha_h = \alpha_{h0}\exp(-\beta_h/E)$[17] along the current path of the substrate current, I_{sub}. Assuming the electric field to decrease linearly from its maximum value E_{db} along the current path of I_{sub}, the current I_{subgen} is expressed as $I_{subgen} \propto I_{sub}(E_{db}/\beta_h)\exp(-\beta_h/E_{db})$, where $E_{db} = \sqrt{2qN_{dep}(\phi_s - V_{bd})/\epsilon_{Si}}$, $\phi_s = 2(kT/q)\log(N_{dep}/n_i)$, N_{dep} is the channel doping concentration, ϵ_{Si} is the dielectric constant of silicon, and n_i is the intrinsic carrier concentration. The vertical electric field, which accelerates electrons of I_{subgen} is determined by the Poisson equation $dE/dy = qN_{dep}/\epsilon_{Si}$. Approximating N_{dep} to be constant, the vertical electric field linearly depends on the depth as shown in Fig. 4. Integrating the product of the current I_{subgen} and the injection probability p_{inj} along the current path, the gate current by CHISEL injection is expressed as

$$I_{CHISEL} = A_s I_{sub} \left(\frac{E_{db}}{\beta_h}\right)^2 \exp\left(-\frac{\beta_h}{E_{db}}\right) \times \left(\frac{\lambda E_{ym}}{\Phi_{bs}}\right)^3 \exp\left(-\frac{\Phi_{bs}}{\lambda E_{ym}}\right), \qquad (3)$$

where $E_{ym} = \sqrt{2qN_{dep}(\phi_s - V_{bs})/\epsilon_{Si}}$, $\Phi_{bs} \equiv \Phi_b(E_{ox}(0))$ and A_s is a fitting parameter.

Measured and simulated hot-electron gate currents, I_{gd}, are shown in Fig. 5. The proposed model gives proper drain, gate and substrate bias dependence. From the simulated data, CHE is dominant for the total current, $I_{CHE} + I_{CHISEL}$, when the gate voltage is high as shown in Fig. 5 (a). As the gate voltage becomes low, the CHE component has less effect than the CHISEL component, because the electric field in the gate dielectric film near the drain changes from attractive to repulsive which suppresses CHE injection[7][9][16]. The CHE component is independent of the substrate bias, as shown in Fig. 5 (b), because the chanel potential, $V(x)$, and the channel electric field, E_m, are insensitive to the substrate bias. The CHISEL component, on the other hand, increases as the substrate bias goes negative owing to the dependence of E_{db} and E_{ym} on V_{bd} and V_{bs}, respectively.

B. Fowler-Nordheim Tunneling

A gate current in erase mode, I_{gb}, is governed by Fowler-Nordheim (FN) tunneling. We use the BSIM4 gate tunneling current model in accumulation mode[18], I_{gbacc}, to express the FN tunneling current because it is implemented in most simulators for industrial use. The BSIM4 gate tunneling current model is based on FN tunneling model and contains some modification to suit direct tunneling[19]. In the erase bias range, measured tunneling current is well expressed by the BSIM4 gate tunneling current model as shown in Fig. 6.

III. Results and Discussion

Experimental and simulated programming characteristics for 130nm-technology flash memory cells are shown in Fig. 7. The threshold voltage shift, ΔV_{th}, in the simulation is calculated using the shift of floating gate potential and the coupling coefficient. A good agreement is obtained for every control gate voltage. Applying substrate bias improves programming efficiency and leads to shorter programming time owing to CHISEL injection, which is properly expressed by our model.

Erasing characteristic is also simulated and compared with experimental data in Fig. 8. A good agreement is obtained for every control gate voltage using common BSIM4 model.

The simulation results of both programming and erasing indicate that our model is useful in designing and optimizing circuits including flash memory cells.

IV. Conclusion

We have proposed a compact model for flash memory cells including a substrate-bias-dependent hot-electron gate current model. The hot-electron gate current model is based on the lucky-electron model, and substrate bias dependence is properly incorporated in it. The tunneling gate current is expressed by the BSIM4 tunneling gate current model. Simulation results of both programming and erasing characteristics have been shown to validate our model.

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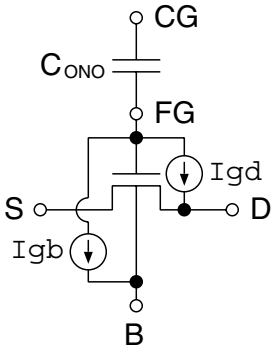


Fig. 1. Equivalent circuit for a flash memory cell.

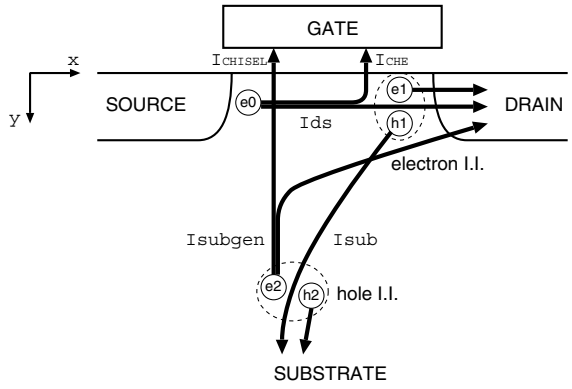


Fig. 2. Schematic diagram of generation mechanisms of gate current during programming. CHE and CHISEL components correspond to $I_{\rm CHE}$ and $I_{\rm CHISEL}$, respectively.

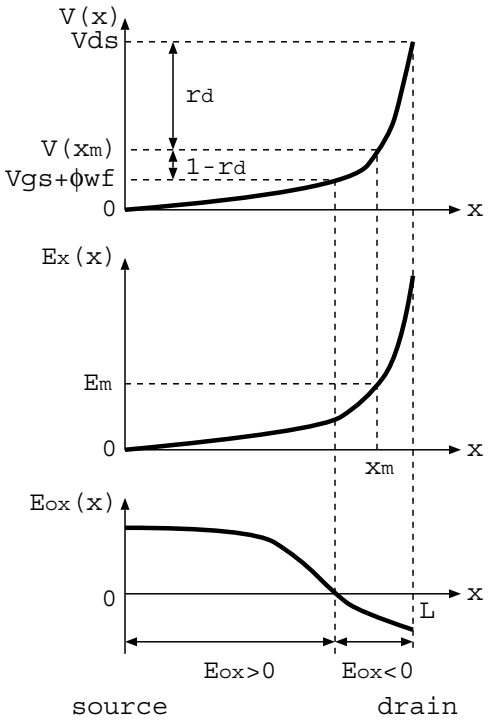


Fig. 3. Schematic diagram of the channel potential, $V(x)$, the electric field along the channel, $E_x(x)$, and the vertical electric field in the gate insulator, $E_{\rm ox}(x)$ along the channel direction.

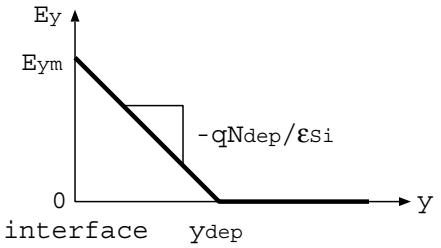
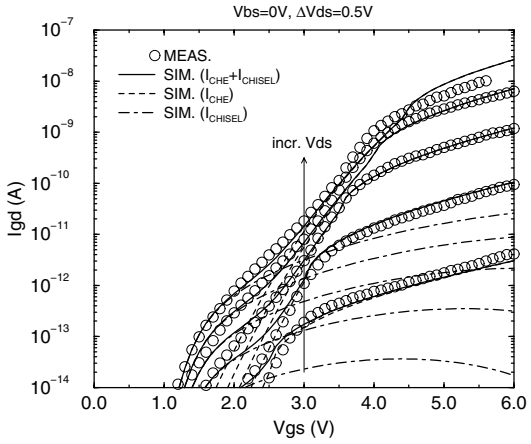
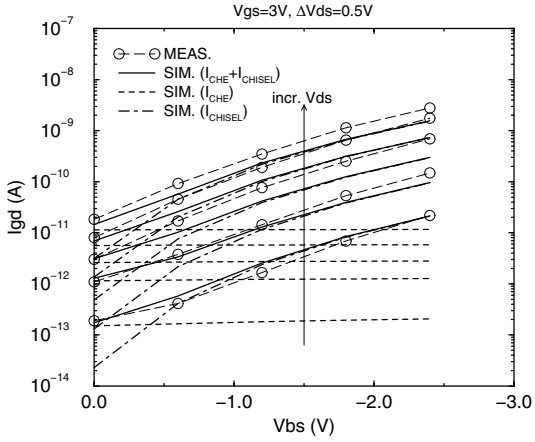


Fig. 4. Schematic diagram of the vertical electric field in the silicon substrate.



(a) $I_{\rm gd}$-$V_{\rm gs}$ characteristics.



(b) $I_{\rm gd}$-$V_{\rm bs}$ characteristics.

Fig. 5. Measured and simulated hot-electron gate current. Measured current is obtained by differenciating measured programming characteristics with time.

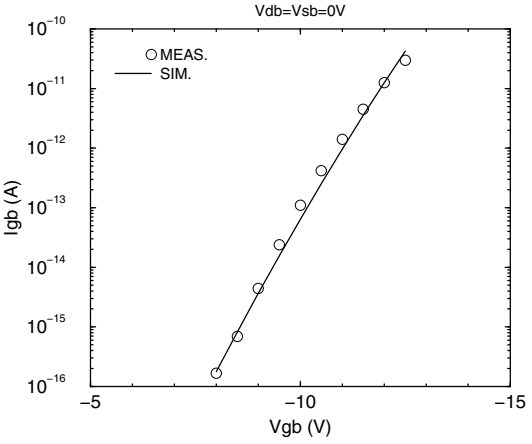
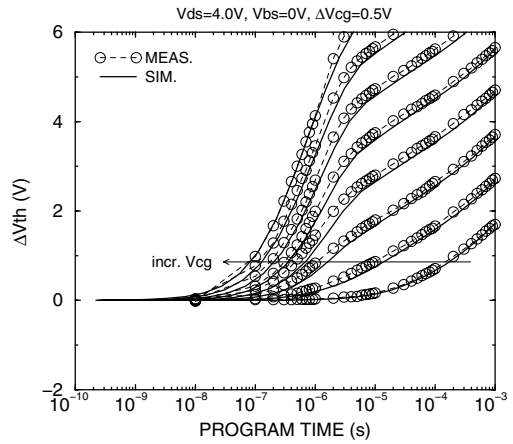
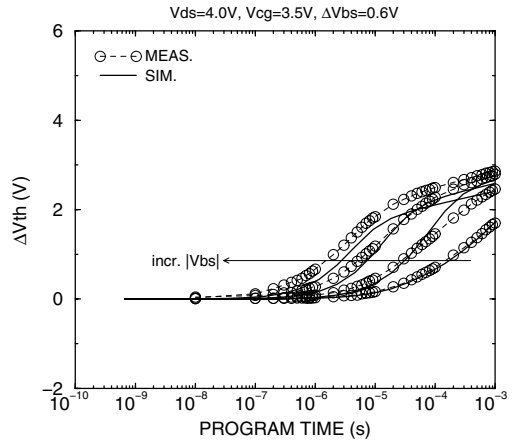


Fig. 6. Measured and simulated tunneling gate current. Measured current is obtained by differenciating measured erasing characteristics with time.



(a) Control gate bias dependence.



(b) Substrate bias dependence.

Fig. 7. Programming characteristics.

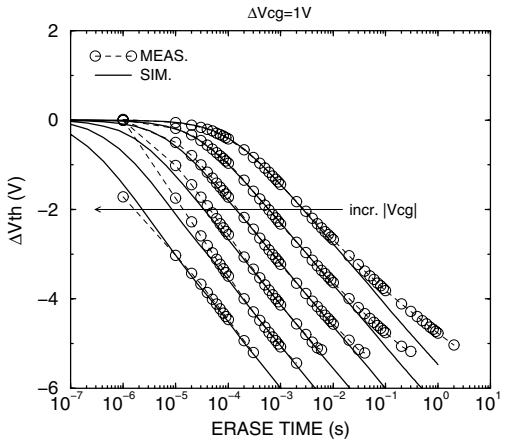


Fig. 8. Erasing characteristics.