Study on Cell Characteristics of PRAM using the Phase–Change Simulation

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***Abstract*—In this paper, we present a new simulation methodology for analyzing cell characteristics of the chalcogenide based phase-change device, PRAM (Phase-change Random Access Memory), which is the future-generation non-volatile memory. Using the new simulation methodology, we analyze the effect of process variation, which is the most sensitive factor to operate the cell of PRAM.**

Keyword: PRAM, phase change simulation, Chalcogenide, Joule's heating, Crystallization model, CFD-ACE

I. INTRODUCTION

The PRAM based on chalcogenide material, known as OUM, has demonstrated a possibility as a promising future memory technology [1-3]. A simulation methodology for this new concept device is strongly required because of the necessity of various process modifications for the low-power and high-performance device realization. Even though several research groups have studied the phase-change mechanism of the chalcogenide material used in an optical device, the quantitative analyses for the electronic memory applications have been still rare. In this paper, we have developed the simulation environment for analyzing the cell characteristics of PRAM, in which the thermal analysis to consider Joule's heating is applied to the phase-change modeling of the chalcogenide. Based on the new simulation methodology, optimal SET conditions ensuring the stable sensing are obtained for the specific RESET condition. The cell failure probability due to PVT(Process, Voltage and Temperature) variation is studied by applying the Monte Carlo method. In the future, it is possible to obtain the optimal process condition using the proposed methodology.

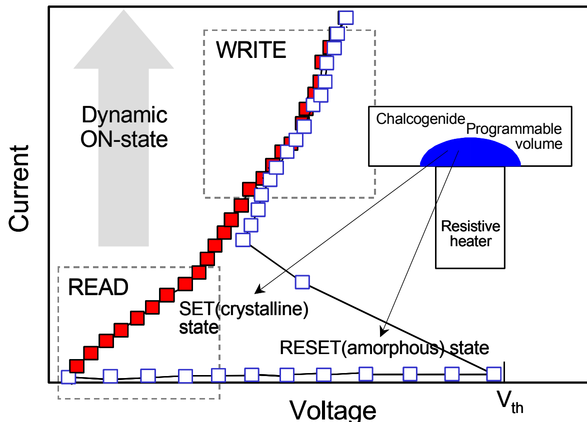

Figure 1. I-V characteristics of a PRAM memory cell. Inset figure depicts the bottom contact of the cell structure.

II. PHASE-CHANGE SIMULATION

As shown in Fig. 1, the write and read of the memory cell, including SET and RESET operations, are operated at the different I-V region. The write operation is performed at the dynamic on-state over V_{th}(threshold voltage) while the read operation is done at the low current level [5]. Therefore, the overall simulation flow is designed to separately treat the write and read operations, as shown in Fig. 2. The flow consists of three major parts - heat generation simulation, modeling of the crystallization process, and cell resistance calculation for the given chalcogenide crystal fraction.

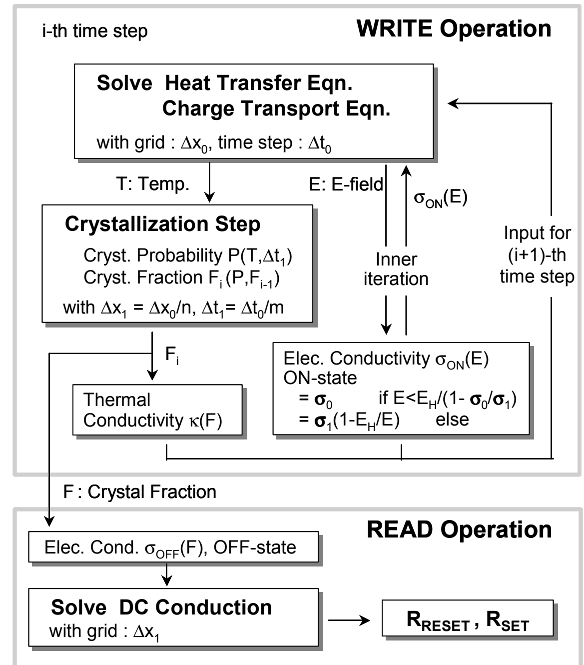

Figure 2. The overall flow of phase-change simulation. F_W is an average crystal fraction for neighboring cells.

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A. *Heat generation simulation*

As the heat generation mechanism is Joule's heating, the DC current source is applied. Heat generation between contact and chalcogenide and the propagation through adjacent material, as shown in Fig. 3, are analyzed by solving the heat transfer equation with convection and adiabatic boundary condition. From the temperature profile by heat generation, the phase-change phenomena are simulated that chalcogenide melts over 889K and crystallizes between 473K and 889K.

B. *Modeling of the crystallization process*

Crystallization is classified into nucleation type formed by the nuclei growth and the growth type which is effected by degrees of crystallization of adjacent cells. Fig. 4 shows the probabilities of each type of crystallization.

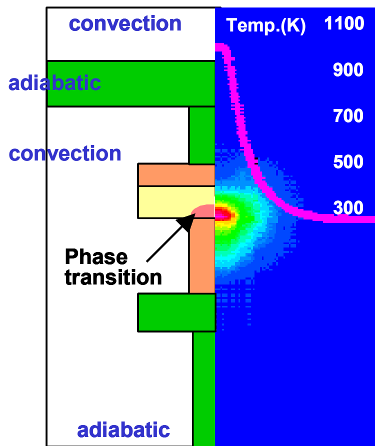


Figure 3. Simulation of temperature profile

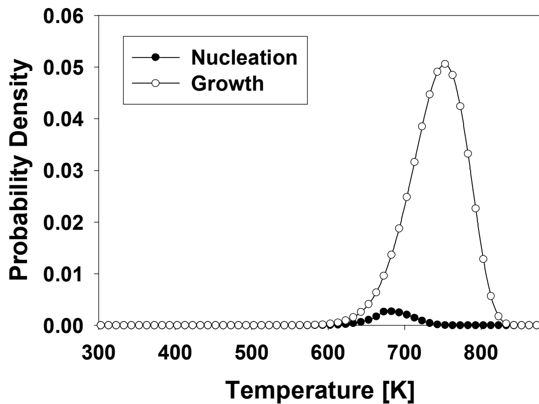


Figure 4. Temperature dependence of crystallization probabilities of nucleation and growth types.

TABLE I. MATERIAL PARAMETERS. GST IS $Ge_2Se_2Te_5$.

Material	Electrical Conductivity. σ (1/Ω-m)	Density (g/㎤)	Thermal Conductivity. κ (J/㎝-K-s)	Specific Heat (J/㎤ -K)
GST	Ref. Fig.5	6.2	Ref. Fig.5	1.2
W	1.75E7	19.3	1.78	2.58
TiN	1.0E6	5.4	0.13	3.235
SiO2	1.0E-14	2.33	0.014	3.1

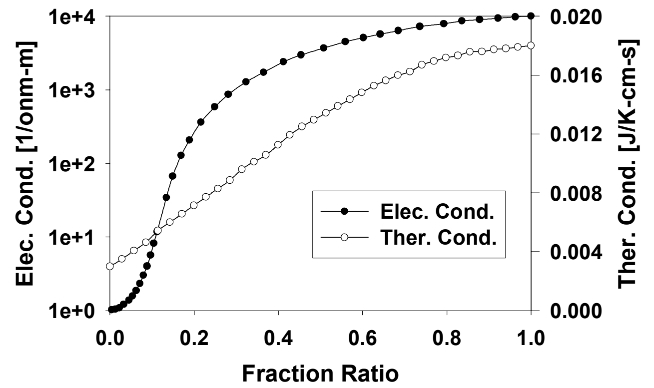
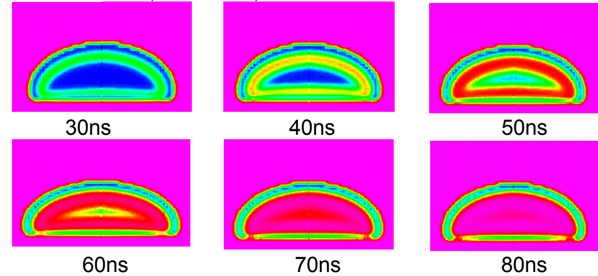


Figure 5. Electrical and thermal conductivities of the chalcogenide material, $Ge_2Se_2Te_5$, as a function of crystal fraction.



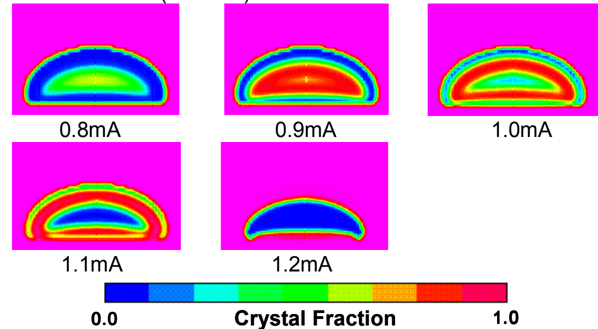


Figure 6. Crystallization of chalcogenide caused by Joule heating. (a) Time evolution of crystallization, (b) Fraction profiles for different SET currents.

The crystallization probabilities are calculated at each transient time step, as a function of temperature and time step Δt. Crystal fraction F_i of specific grid cells at i-th time step is determined by following equation.

$$F_i = F_{i-1} + (F_w \times P_g + P_n) \times (1-F_{i-1}) \quad (1)$$

F_{i-1} is the crystal fraction of the previous time step and F_w is the sum of crystallization of nearest neighboring cells. Crystal fraction 1 and 0 mean crystalline and amorphous phases, respectively. To exactly simulate phase-change, 2 nm and 0.1 ns are used for fine grid Δx_1 and time step Δt_1, respectively. The crystallization probability includes both growth and nucleation terms and their magnitudes are verified experimentally, as shown in Fig. 4 [4]. The fraction dependence of electrical and thermal conductivities of

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chalcogenide is considered, as shown in Fig. 5. The material parameters are summarized in Table I.

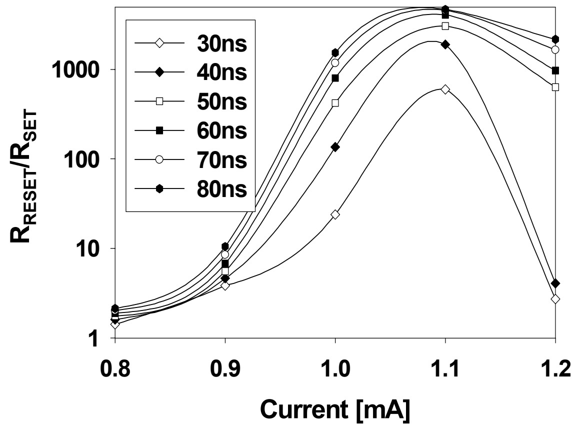

Figure 7. R_{RESET}/R_{SET} for various SET currents and pulse widths (D_{BC}=80nm, I_{RESET}=1.5mA, t_{RESET}= 10 ns).

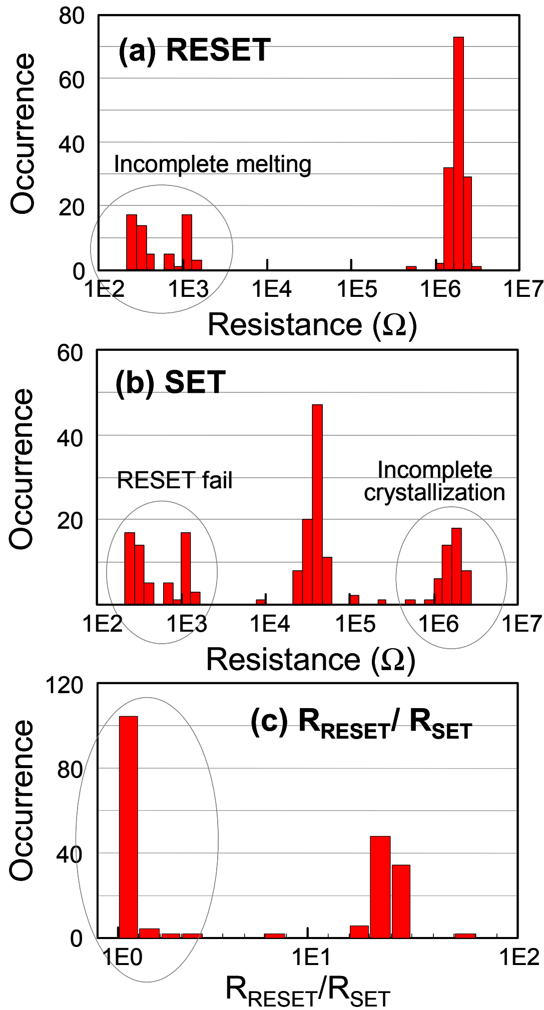

Figure 8. Distributions of cell resistances after (a) RESET and (b) SET operations. (c) The distribution of R_{RESET}/R_{SET}.

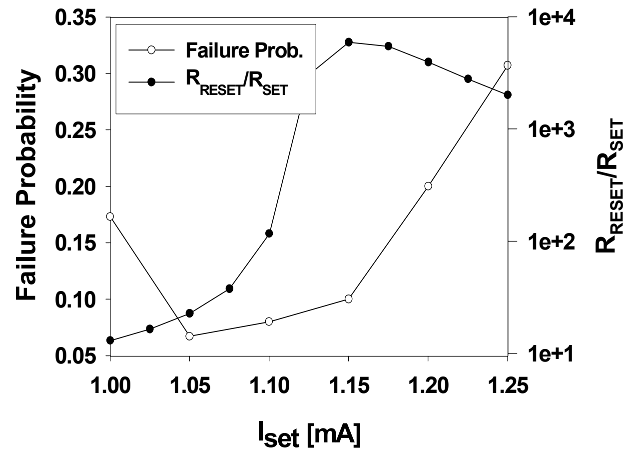

Figure. 9. The cell failure probability and resistance ratio (R_{RESET}/R_{SET}) as a function of I_{SET}.

C. Cell resistance calculation

Cell resistance is simulated in read the operation module. In this case, the crystal fraction generated by write operation is used as an input for all of cells inside chalcogenide and the electrical conductivity is substituted with values in Fig. 5. Resistance is calculated by applying the micro-level current which do not cause the phase-change.

III. SET OPERATION AND CRYSTALLIZATION

Basic characteristics of the SET operation are examined using the proposed simulation flow. Fig. 6(a) shows the evolution of crystallization during the SET operation. It exhibits clearly that the crystallization begins at the region slightly below the surface of the melted volume in RESET and propagates into the inner region. The outer shell remains in the mixed phase of amorphous and crystalline states. Fig. 6(b) shows degrees of crystallization for different SET currents. Resistance ratios of RESET and SET states for difference SET currents and pulse widths are plotted in Fig. 7. The resistance ratio exhibits the maximum at the specific SET current, since the crystallization probability gets smaller at the higher temperature and the SET becomes similar to the RESET operation. In addition, the ratio is saturated as the SET time increases. From this simulation results, we can find the optimal SET current for the specific RESET current.

IV. CELL FAILURE ANALYSIS

For the first time, we have applied the Monte Carlo method and obtained the cell failure occurrence as functions of operation parameters and amounts of variation.

A. Process Variations

Most sensitive parameters - diameter of the bottom contact (D_{BC}) and write currents (I_{SET}, I_{RESET}) - are assumed to be in the Gaussian distribution with given variances. Fig. 8 shows the distributions of the cell resistance after the RESET and SET operations. The cell failure can be classified into RESET and SET fails because of the incomplete melting and crystallization, respectively. Fig. 9 shows the failure

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probability as a function of I_{SET} which is compared with the resistance ratio. It is obvious that the I_{SET} maximizing the RESET/SET resistance ratio is not optimal from the cell failure viewpoint. The I_{SET} should be determined to minimize the cell failure probability; thus, it is smaller than the value for the maximum resistance ratio. Fig. 10 exhibits that the failure probability is more sensitive to D_{BC} and 3σ–variations of D_{BC} and write currents should be less than 10%. Therefore, the results clearly demonstrate that PRAM is significantly sensitive to the process variations and their control is very important.

B. Temperature Dependency

Fig. 11 shows the experimental results of real PRAM devices. The temperature dependence of fail bit counts is changed as I_{SET} is changed. As shown in Table II, our simulation results for the temperature dependence considering the process variations show very similar trends with experiments. The number of RESET fails decreases at the higher temperature, regardless of I_{SET}. On the other hand, the SET failure shows different temperature dependences for different I_{SET}'s, since the crystallization probability has a maximum at the certain temperature below the melting point. It is definitely formidable to control cell characteristics at all temperature range simultaneously, which is the major challenge in future PRAM development.

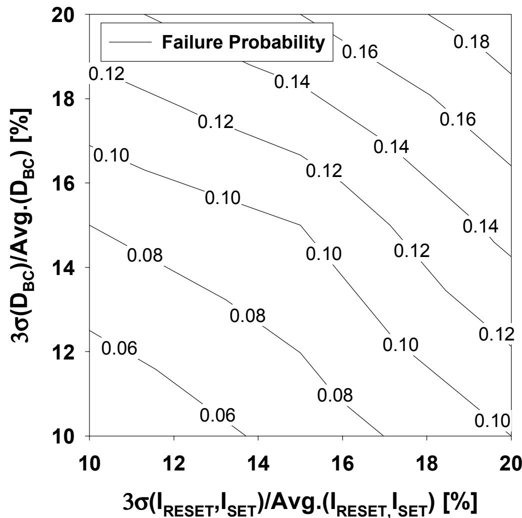

Figure 10. Failure probability for various variances of D_{BC}, I_{RESET}, and I_{SET}. Mean values of D_{BC}, I_{RESET} are 80 nm and 1.6 mA. t_{RESET} = 30ns, t_{SET} = 80 ns.

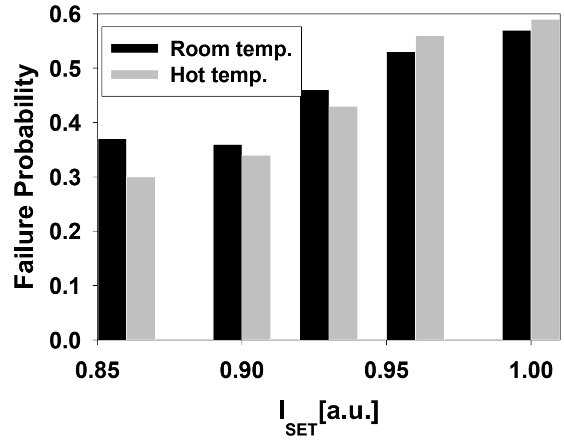

Figure 11. Measured cell failure probability for the real PRAM device .

IV. CONCLUSION

We have analyzed the sensitivity of PRAM characteristics to process and temperature variations by applying a new phase-change simulation method. Cell failure analysis clearly demonstrates that PRAM is very sensitive to process and temperature variations and their control would be one of major challenges in future device development. Measured temperature dependence of failure characteristics is well explained by our theoretical investigation.

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TABLE II. TEMPERATURE DEPENDENCY OF CELL FAILURE OCCURRENCE USING SIMULATION. THE NUMBER OF FAIL BITS IS OBTAINED WITH VARYING THE TEMPERATURE AND SET CURRENT WITH TOTAL 200 BITS. MEAN VALUES OF D_{BC}, I_{RESET} ARE 80 NM AND 1.7 MA. T_{RESET} = 40NS, T_{SET} = 100 NS. 3σ-VARIAITONS OF D_{BC}, I_{RESET}, AND I_{SET} IS 15% OF THEIR MEAN VALUES.

	Number of fail bits among 200 bits								
I_{SET} (μA)	**1030**			**1060**			**1100**		
Temp. (°C)	-30	27	85	-30	27	85	-30	27	85
RESET Fail	2	1	0	2	1	0	2	1	0
SET Fail	14	4	5	2	6	9	5	12	20
Total Fail	16	5	5	4	7	9	7	13	20

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