Implications of Gate Design on RF Performance of Sub-100nm Strained-Si/SiGe nMODFETs

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Abstract

The effects of gate structure design on RF performance of strained-Si/SiGe nMODFETs are studied using device simulation and experiments. It is found that while gate resistance only affects f_{max}, fringing gate capacitance can have a significant impact on both f_T and f_{max}, indicating that the physical gate structure has to be optimized for any specific application. The experiments suggest that low-κ material is needed as sidewall spacer (if any) and passivation for reducing fringing gate capacitance. Furthermore, the simulations show that if low gate resistance can be achieved by using a multi-finger geometry, a rectangular-shaped gate should be used in order to reduce fringing gate capacitance. If not, a T-gate should be used to reduce gate resistance for high f_{max}.

Introduction

Strained Si/SiGe nMODFETs with high electron mobility are potentially promising devices for future RF applications due to expected low power, low noise and high speed [1]. In addition, their compatibility with standard Si CMOS technology offers opportunities for system-on-chip applications. It has been shown that proper device scaling is needed for MODFETs to achieve higher performance [2]. In this paper, we report a systematic simulation study on the effects of parasitic gate resistance and fringing gate capacitance for the scaled nMODFETs using MEDICI [3].

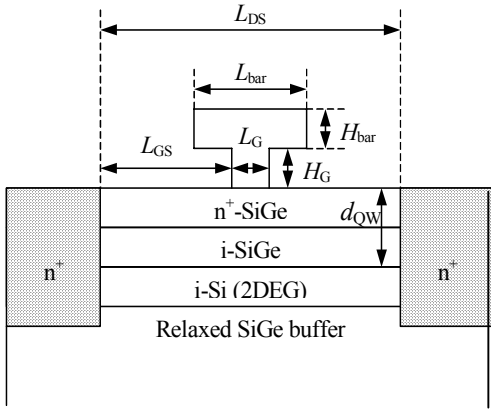

Fig. 1. Schematic of a Si/SiGe nMODFET.

Results and Discussions

Fig. 1 shows the schematic of a MODFET structure. An undoped, tensile strained-Si quantum well channel is on top of a relaxed SiGe virtual substrate. An n-type doped SiGe layer serves as a supply layer, which is formed above the channel with an undoped SiGe spacer layer in between. The gate is a Pt Schottky gate. Three types of gate structures were simulated, a one-dimensional electrode plate for an ideal case of zero fringing capacitance, a rectangular gate with dimensions of L_G x H_G, a T-gate with a foot-print of L_G, a height of H_G, and a "bar" of L_{bar}x H_{bar}.

Fig. 2 and 3 show the SEM pictures of a fabricated T-gate with and without a polymer passivation layer, respectively. Ge content is 25% in the fabricated devices. The devices were measured before and after the removal of the passivation layer in order to study its effects on device performance.

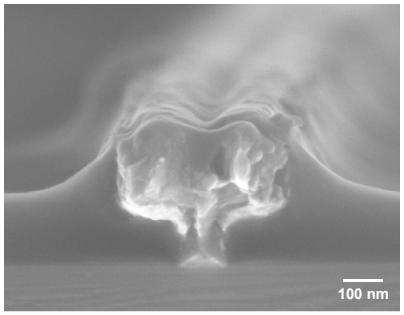

Fig. 2. SEM picture of a T-gate with a passivation layer.

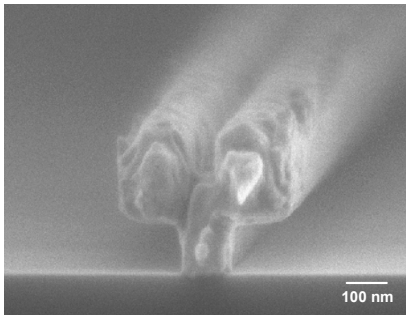

Fig. 3. SEM picture of a T-gate without the passivation layer.

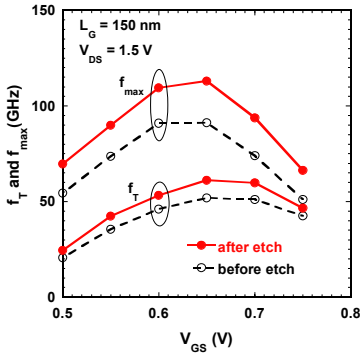

Fig. 4. Measured f_T and f_{max} vs. V_{GS} for a device with L_G = 150 nm at V_{DS} = 1.5 V before and after the removal of the passivation layer.

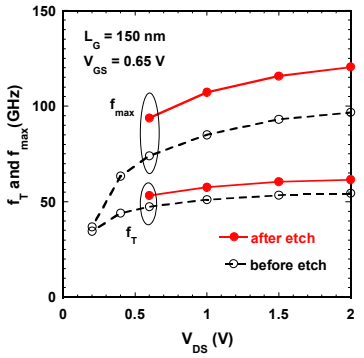

Fig. 5. Measured f_T and f_{max} vs. V_{DS} for the device of Fig. 4 at V_{GS} = 0.65 V.

Fig. 4 and 5 show the measured f_T and f_{max} as functions of applied gate bias and drain bias, respectively, for a device with L_G = 150 nm. While no significant change is observed in the transconductance (g_m), an enhancement of 20% is observed in peak f_T and 35% in f_{max} without the passivation layer. This indicates that the fringing capacitance around the T-gate has a dramatic impact on the RF performance.

Fig. 6 shows a two-dimensional potential contour for a device with L_G = 150 nm at V_{DS} = 1 V and V_{GS} = 0.6 V. The fringing gate capacitance (C_{fringe}) is created by the fringing electric field originating from the T-gate structure. C_{fringe} can be extracted by subtracting the capacitance of the electrode plate (C_{plate}) from the total gate capacitance (C_{GS}). Fig. 7 shows the simulated f_T and C_{GS} versus gate bias for the device of Fig. 6, having various passivation materials, i.e., air, a certain type of polymer, oxide and nitride. f_T decreases while C_{GS} increases substantially with permittivity increasing. Therefore, it is important to use low-k material as the sidewall spacer and gate passivation.

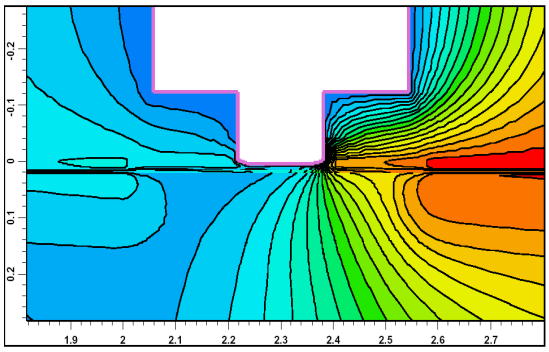

Fig. 6. Two-dimensional potential contour for a device with L_G = 150 nm at V_{GS} = 0. 6 V and at V_{DS} = 1 V.

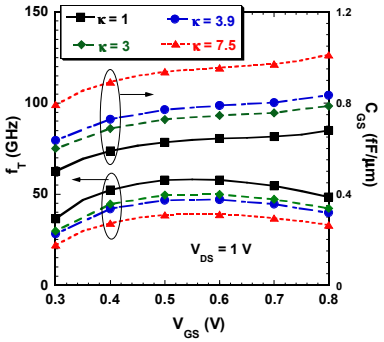

Fig. 7. Simulated f_T and C_{GS} vs. V_{GS} for a device with L_G = 150 nm and various materials for passivation.

Furthermore, in order to achieve high f_T and/or f_{max}, the physical gate structure itself has to be optimized. In the following simulations, SiO_2 was used as the passivation layer and Ge content was 30%. The devices were 50 μm wide. The source/drain series resistance (R_S/R_D) including the contact resistance was assumed to be 3 Ω each. The gate resistance (R_G) is proportional to (W/N), where W is the device width and N is the number of fingers of a multi-finger gate. R_S/R_D and R_G were included in the simulations as lumped elements. First, devices with a 2-finger, rectangular-shaped gate of L_G = 50 nm and various H_G were simulated. Note that R_G was assumed to be proportional to $1/H_G$. However, for the case of electrode plate (H_G= 0), R_G was assumed to be very large (100 Ω) instead of infinite for the purpose of simulation. The calculated R_G values were normalized w.r.t. the case of H_G= 0 and plotted in Fig. 8, together with the normalized gate capacitance. C_{GS} increases dramatically with H_G increasing due to increased fringing capacitance. Fig. 9 shows peak f_T and f_{max} versus H_G. f_{max} increases while f_T decreases with increased H_G. The effects eventually saturate for very large H_G.

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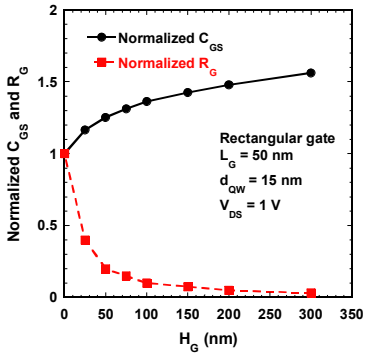

Fig. 8. Calculated R_G and simulated C_{GS} versus H_G for devices with a rectangular gate of L_G = 50 nm at V_{DS} = 1.0 V, both normalized w. r. t. the electrode plate (H_G = 0).

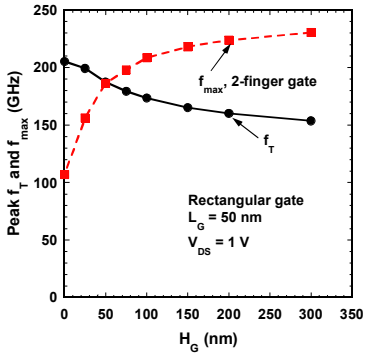

Fig. 9. Simulated peak f_T and f_{max} versus H_G for devices of Fig. 8 with a 2-finger rectangular gate at V_{DS} = 1.0 V.

Second, devices with a T-gate of L_G = 50 nm, H_G = H_{bar} = 100 nm and various L_{bar} were simulated. The minimum value of L_{bar} is L_G, which is 50 nm. On the other hand, L_{bar} cannot be too large for the reason of mechanical stability. Fig. 10 shows the normalized C_{GS} and R_G. Note that R_G was now assumed to be proportional to 1/ L_{bar}. C_{GS} increases with increasing L_{bar} due to increased fringing capacitance created by the "bar", but not as significantly as increased H_G. Fig. 11 shows peak f_T and f_{max} versus L_{bar} for two different sets of R_G. For a given gate dimension, the gate resistance of a single gate was assumed to be 4x higher compared to a 2-finger gate, for the width of the active area only needs to be a half of the width of the single-gate device. f_T decreases with increased L_{bar}, while it does not depend R_G. For the 2-finger gates, f_{max} is not sensitive to L_{bar}. This is because R_G in these devices is already quite small, so the reduction in R_G only partially offsets the reduction in f_T. However, for the single-gate devices, f_{max} improves substantially with increased L_{bar}. This is because R_G in these devices is quite large, and the reduction in R_G overpowers the reduction in f_T. Therefore, for applications that require high f_{max}, a multi-finger, rectangular-shaped gate should be used for achieving low gate resistance and low fringing gate capacitance.

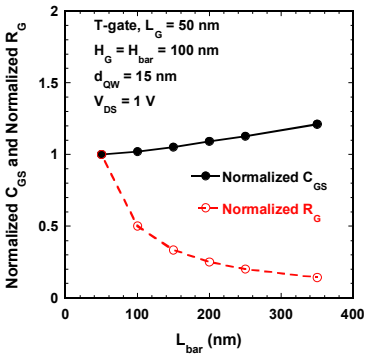

Fig. 10. Calculated R_G and simulated C_{GS} versus L_{bar} for devices with a T-gate of H_G = H_{bar} = 100 nm at V_{DS} = 1.0 V, both normalized w. r. t. a rectangular gate (L_{bar}=L_G = 50 nm).

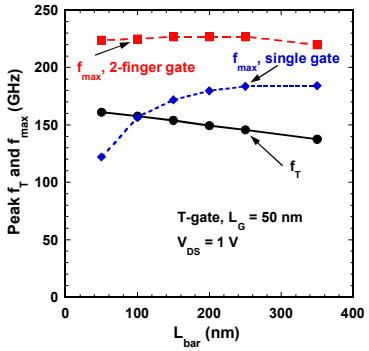

Fig. 11. Simulated peak f_T and f_{max} versus L_{bar} for devices of Fig. 10 with a 2-finger T-gate and a single T-gate at V_{DS} = 1.0 V.

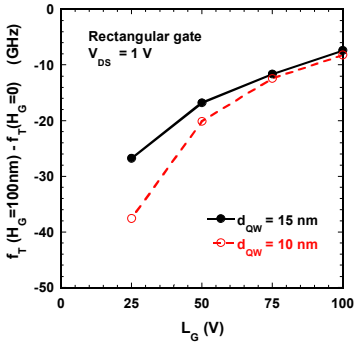

Fig. 12. Simulated relative peak f_T versus L_G for devices with rectangular gate H_G = 100 nm, d_{QM} = 10 and 15 nm at V_{DS} = 1.0 V.

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Fig. 12 shows the percentage decrease of peak f_T as a function of L_G for devices with a rectangular gate of H_G = 100 nm. A more severe decrease is observed for the devices with a shallower quantum well (d_{QW} = 10 nm) compared to d_{QW} = 15 nm, especially at a shorter gate length. Therefore, the gate design becomes even more important as MODFETs are further scaled.

Conclusions

In summary, device simulations and experiments were performed to investigate the effect of fringing gate capacitance and parasitic gate resistance on RF performance of sub-100 nm Si/SiGe nMODFETs. It is shown that the fringing capacitance has a huge impact on both f_T and f_{max}, while gate resistance only affects f_{max}. The effect becomes more significant for sub-100 nm nMODFETs with a shallower quantum well. Low-κ material should be used as passivation and the gate structure design has to be carefully carried out in order to achieve high RF performance.

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