Maximum Drive Current Scaling Properties of Strained Si NMOS in the Deca–Nanometer Regime

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***Abstract*— The scaling of the drive current of strained Si NMOSFETs with gate lengths from 250nm down to 50nm is investigated with the self-consistent full-band Monte Carlo model. Although a degradation of the performance improvement due to strain is observed for decreasing gate length, this effect seems to saturate at very short channel lengths because of quasi-ballistic transport effects. For a gate length of 50nm still an improvement of the drive current of more than 30% is found for Ge concentrations in the substrate of more than 15%.**

I. Introduction

Recently, it has become clear that strained Si (SSI) will play an important role for next–generation CMOS processes [1]–[3]. Very significant performance advantages of SSi NMOS devices in comparison to their unstrained Si (USI) counterparts have been reported especially in terms of maximum drive current [3], [4] even for devices with sub–100 nm channel lengths. Therefore, the scaling behavior of SSi NMOS devices with deca–nanometer channel lengths is very important and especially maximum drive current scaling is of interest [5].

Full-Band Monte Carlo (FBMC) device simulation is currently the most accurate method to study these questions and in Ref. [6] transport in a SSi NMOSFET with a metallurgical channel length of $100\mathrm{nm}$ has been investigated. In this work devices with different metallurigcal channel lengths down to $25\mathrm{nm}$ are simulated to investigate the scaling behavior of SSi NMOSFETs. In contrast to Ref. [7], where nonself-consistent FBMC simulations were used, which are not reliable in the deca-nanometer regime [8], here the investigation is based on self-consistent FBMC simulations [9], [10].

II. Results

The simulations are performed with the FBMC simulator ELWOMIS [9], [10], where the band structures are calculated by the nonlocal empirical pseudopotential method [11]. In the case of SSi the only change compared to the USi model is in the band structure. The scattering models remain the same and good agreement with experimental results for the phonon-limited low-field mobility in SSi [12] is obtained without any parameter matching (Fig. 1).

In the case of a MOSFET the drive current is mainly determined by the transport in the inversion layer and in Fig. 2 the low-field mobility is shown for effective fields found in modern short-channel devices. The USi results agree well with measured data [13]. The SSi results saturate for Ge contents larger than 15%. The channel velocity is shown in Fig. 3 and the saturation velocity is not affected by the strain. Thus, it is not clear to which extend strain will improve the performance of deep sub-micron devices, in which the driving channel fields are rather large.

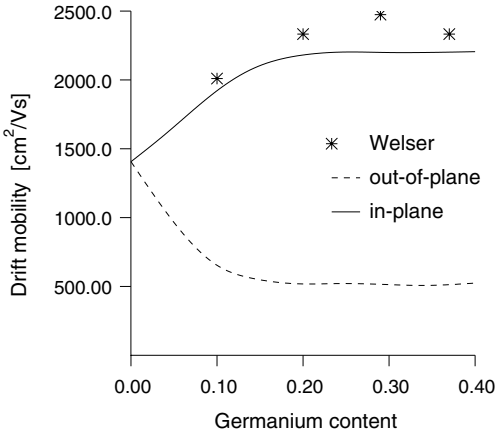

Fig. 1. Bulk mobility for undoped SSi at room temperature and experimental results [12].

In order to investigate this question, devices with different gate lengths are simulated (Fig. 4, Tab. I), which are scaled with a constant off-current of about $0.1\mathrm{nA}/\mu\mathrm{m}$ ($0.01\mathrm{nA}/\mu\mathrm{m}$ for the shortest device). The doping profile of the shortest gate length device is similar to the one of Ref. [14], whereas the other devices have a homogeneously doped bulk. For the sake of an easier comparison the SSi devices are simulated assuming that the whole bulk consists of SSi. Simulations including the SiGe substrate showed no significant differences. Since the strain changes the Si workfunction, the threshold voltage changes with strain. To account for this effect, the gate voltages of the SSi MOSFETs are reduced in such a way that the same inversion density in the channel is obtained for a low drain/source bias regardless of the strain (Fig. 5) [6].

The on-current versus gate length is shown in Fig. 6 and a decrease in the gain is observed for smaller gate lengths due to the increase of the driving field in the channel. On the other

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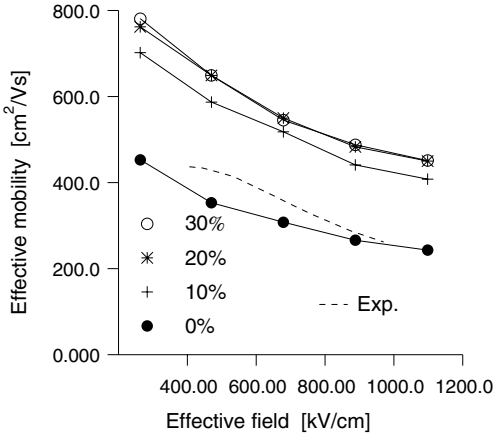

Fig. 2. Effective low-field mobility of electrons in an inversion layer at room temperature and a homogeneous bulk doping of $10^{17}/\mathrm{cm}^3$ as a function of the Ge content of the virtual relaxed SiGe layer and measured data for a bulk doping of $3 \cdot 10^{17}/\mathrm{cm}^3$ [13].

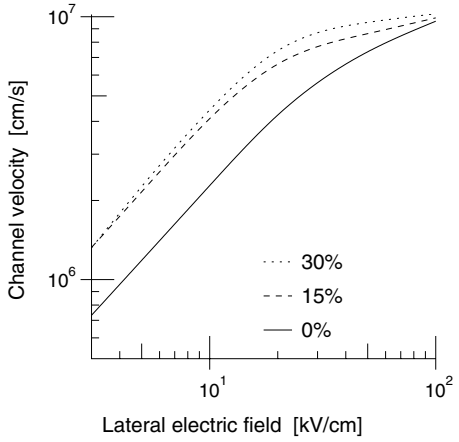

Fig. 3. Effective drift velocity of electrons in an inversion layer at room temperature, a homogeneous bulk doping of $10^{17}/\mathrm{cm}^3$, and an effective field of $1100\mathrm{kV/cm}$ as a function of the Ge content of the virtual relaxed SiGe layer.

hand, for the two shortest gate lengths no further decrease is found. A similar behavior is found in the case of the $50\mathrm{nm}$ device as a function of the drain voltage (Fig. 7), where the gain is still larger than 30%.

This favorable scaling behavior is in contrast to the simple argument used above that the increasing driving field in the channel reduces the gain with decreasing channel length. A more sophisticated theory for the on-current of MOSFETs based on thermionic injection over the potential barrier at the source side of the channel was presented in Ref. [15]. The potential at the Si/SiO_2 interface is shown for the shortest device in Fig. 8 and the peak of the barrier is located at $-8\mathrm{nm}$. The injection velocity (the average velocity of all particles moving towards the drain not counting particles going backwards) increases with strain (Fig. 9). Moreover, the injection velocity at the peak of the barrier is increased by about 50% compared to its value in the source, where the particle gas is closer to equilibrium. The mean velocity of the

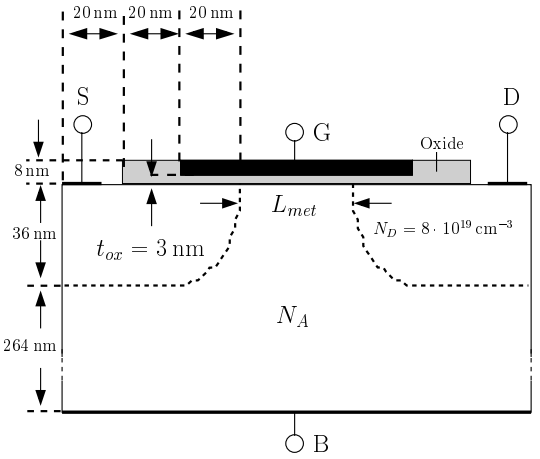

Fig. 4. Geometry of the NMOSFETs.

TABLE I
GEOMETRY AND CHANNEL DOPING OF THE SIMULATED NMOS DEVICES.

L_{gate} [nm]	L_{met} [nm]	N_{A} [cm^{-3}]	Structure
50	25	$5.0 \cdot 10^{18}$	Taur et al. [14]
80	40	$2.2 \cdot 10^{18}$	Fig. 4
100	60	$1.2 \cdot 10^{18}$	Fig. 4
130	90	$7.0 \cdot 10^{17}$	Fig. 4
180	140	$4.0 \cdot 10^{17}$	Fig. 4
250	210	$3.3 \cdot 10^{17}$	Fig. 4

back-scattered particles on the other hand is reduced at the peak position resulting in 40.3% back-scattering flux in the USI case, 32.7% for 15% Ge, and 31.6% for 30% Ge. This is due to the reduced scattering in the strained case.

A reduction in scattering and a higher velocity due to strain should increase the mean free path of the electrons in the inversion layer. According to Ref. [16] the vector mean free path is given by the average of the microscopic relaxation time times velocity. In Fig. 10 the component of the mean free path in the channel direction is shown, where surface scattering was accounted for in a heuristic way. In the source the mean free path is very small because of the randomized velocity of the particles. When the particles enter the channel their average velocity in the direction of the channel and therewith mean free path increases. At the injection point the mean free path is $2.5\mathrm{nm}$ for USi, $3.2\mathrm{nm}$ for 15% Ge, and $3.4\mathrm{nm}$ for 30% Ge in the substrate. Thus, the mean free path at the injection point is still much smaller than the channel length of the devices. The maximum of the mean free path is found in the middle of the channel, beyond which the increase in scattering is stronger than the gain in velocity and the mean free path becomes smaller.

In Fig. 11 the resultant channel velocity and density is shown. In the case of the SSi devices a first velocity overshoot peak is found close to the peak of the mean free path. Since the particle density on the source side of the channel is

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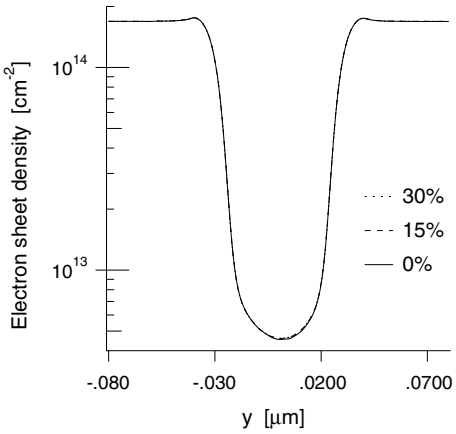

Fig. 5. Electron density integrated perpendicular to the channel direction for the 80nm devices biased at $V_{\text{gate}} = 1.5\text{V}$ (unstrained Si) and $V_{\text{drain}} = 0.1\text{V}$.

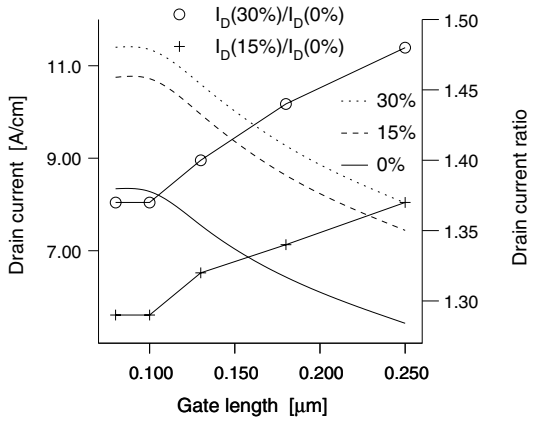

Fig. 6. On-current of the NMOSFETs biased at $V_{\text{gate}} = 1.5\text{V}$ (unstrained Si) and $V_{\text{drain}} = 1.5\text{V}$.

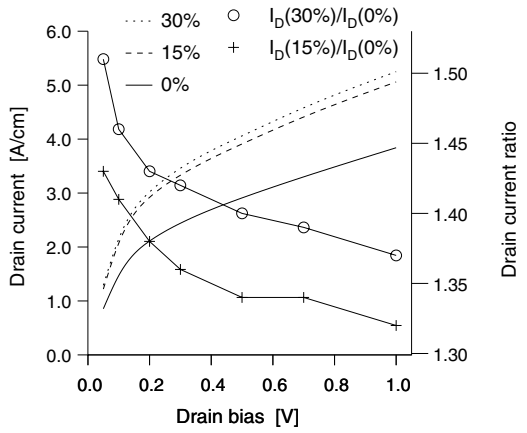

Fig. 7. Drain current of the 50nm NMOSFET biased at $V_{\text{gate}} = 1.0\text{V}$ (unstrained Si).

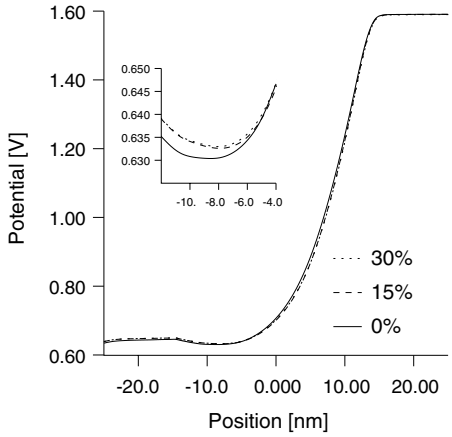

Fig. 8. Electrostatic potential close to the oxide for the 50nm NMOSFET biased at $V_{\text{gate}} = 1.0\text{V}$ (unstrained Si) and $V_{\text{drain}} = 1.0\text{V}$.

almost independent of the strain, the higher velocity at the injection point leads to the larger on-current. It is worth noting that in the SSi case the velocity at the peak of the barrier is larger than 65% of the saturation velocity. Moreover the average electron temperature (Fig. 12) at the peak position of the barrier is larger than the lattice temperature but much smaller than the electron temperature which is observed under homogeneous conditions at 65% of the saturation velocity. Both observations imply quasi-ballistic transport and strong nonequilibrium effects at the peak of the barrier.

III. Conclusion

FBMC simulations predict that SSi NMOS devices will improve the maximum drive current even for NMOS devices with deca–nanometer channel lengths by more than 30 %. This shows that SSi MOSFETs have favorable scaling properties in the deca–nanometer regime, which are due to a favorable velocity overshoot behavior at the source side of the channel in SSI MOSFETs.

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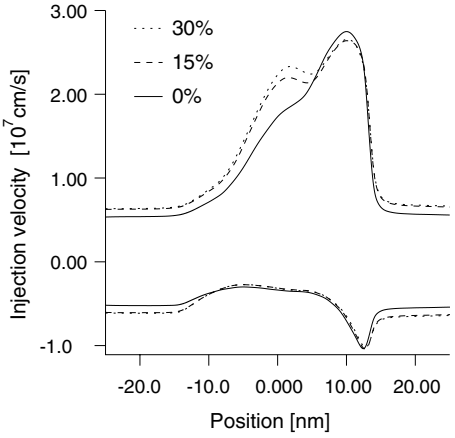

Fig. 9. Average positive and negative electron velocity parallel to the direction of the channel for the $50\mathrm{nm}$ NMOSFET biased at $V_{\text{gate}} = 1.0\mathrm{V}$ (unstrained Si) and $V_{\text{drain}} = 1.0\mathrm{V}$.

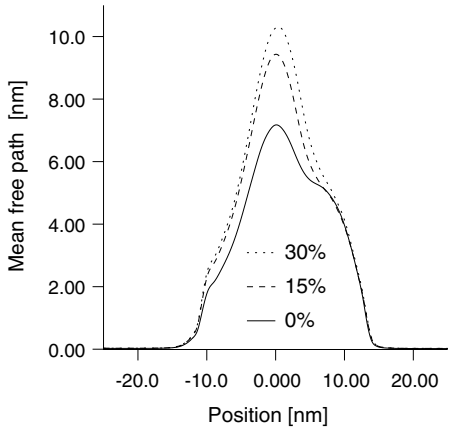

Fig. 10. Average mean free path in the direction of the channel for the $50\mathrm{nm}$ NMOSFET biased at $V_{\text{gate}} = 1.0\mathrm{V}$ (unstrained Si) and $V_{\text{drain}} = 1.0\mathrm{V}$.

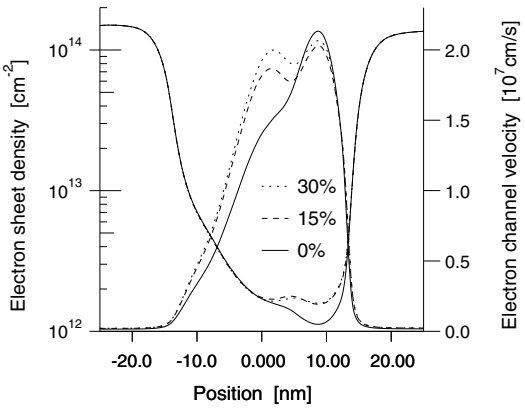

Fig. 11. Electron density integrated perpendicular to the channel direction and average channel velocity for the $50\mathrm{nm}$ NMOSFET biased at $V_{\text{gate}} = 1.0\mathrm{V}$ (unstrained Si) and $V_{\text{drain}} = 1.0\mathrm{V}$.

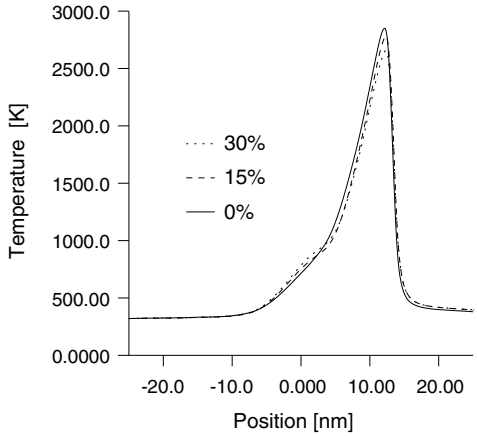

Fig. 12. Average electron temperature for the $50\mathrm{nm}$ NMOSFET biased at $V_{\text{gate}} = 1.0\mathrm{V}$ (unstrained Si) and $V_{\text{drain}} = 1.0\mathrm{V}$.

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