Optimization of Sub-50nm MOSFETs to Mitigate Drive Current Degradation Due to Silicon Recess in S/D

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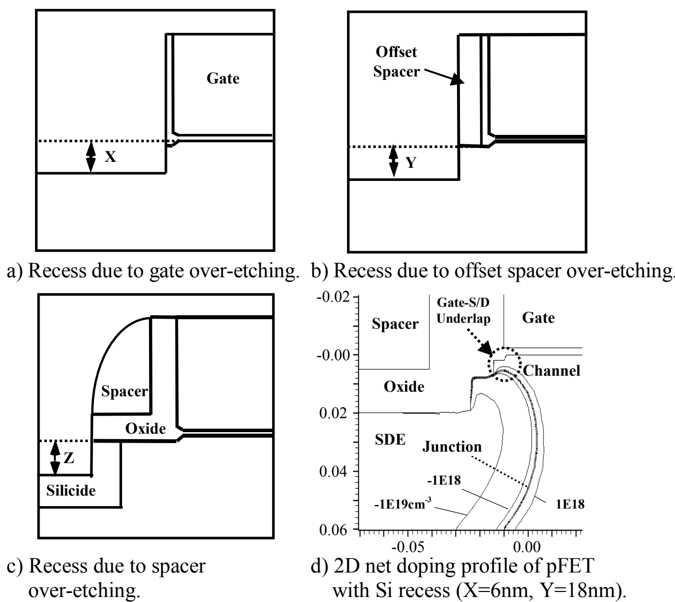
Abstract—**The recess of silicon in the source/drain and extension area severely compromises the performance of sub-50nm MOSFETs. In this paper we investigate the influence of silicon recess on the transistor characteristics using process and device simulation, and systematically map the engineering space for optimization of channel, halo, S/D implants, spacer formations, silicidation and integration schemes to mitigate the silicon surface gouging using response surface modeling.**

Keywords-component; MOSFETs; silicon recess; transistor design; halo; S/D extension; silicide; SOI film thickness; process simulation; device simuilation; response surface model

I. INTRODUCTION

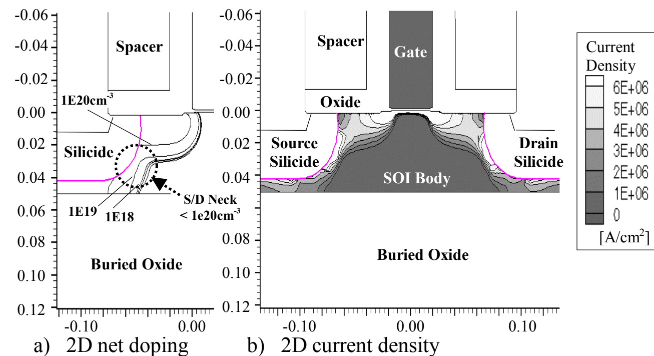
First of all, we have to inquire into the mechanism of drive current degradation due to silicon recess in Source/Drain (S/D). Non-optimized dry etching and reactive cleans can potentially recess silicon region during processing. Depending on the details of gate and spacer processing, three types of silicon recess can be introduced, as shown in Fig.1a-c. The S/D Extension (SDE) implant with 0° tilt angle and the high dose tilted halo implant into the SDE recess causes the gate-S/D underlap which leads to lower gate-S/D overlap capacitance (Cgd) but higher series resistance between channel and SDE (Fig.1d) [1].



a) Recess due to gate over-etching. b) Recess due to offset spacer over-etching.

c) Recess due to spacer over-etching. d) 2D net doping profile of pFET with Si recess (X=6nm, Y=18nm).

Fig. 1: Over-Etching which may cause Si recess.



a) 2D net doping b) 2D current density

Fig. 2: Simulated 2D net doping and current density profiles of 40nm-gate SOI nFET with Tsoi=50nm. Vd=Vg=1.0V.

The Si-silicide interface moves down with increasing depth of Si recess. Deepening the Si-silicide interface gives rise to the high series resistance at S/D neck region and the current crowing in S/D, especially for SOI MOSFETs (Fig.2). We here discuss the transistor design to suppress the influence of silicon recess along with optimized channel, halo, S/D and silicide for high performance transistor applications.

II. TRANSISTOR DESIGN

Our transistor design scheme falls roughly into four steps (table1). These assume that the gate length, gate oxide thickness, supply voltage and off-current (Ioff) have already been established for a technology node. The first step of high performance transistor design is to decide the junction depth (Xj) and lateral abruptness of SDE appropriate for a technology node. The energy and dose of Pre-Amorphization Implant (PAI) and SDE implant, and the temperature, time and ramp rate of S/D Rapid Thermal Anneal (RTA) should be optimized to achieve a target Xj and lateral abruptness with high activation.

III. MINIMIZATION OF GATE-S/D OVERLAP

Next, the gate-S/D overlap capacitance should be minimized while avoiding the significant increase in series resistance at S/D overlap region, by optimizing the gate notch or the offset-spacer [2][3]. The transistor characteristics become very sensitive to the depth of silicon surface gouging when the gate-S/D overlap distance is minimized. Fig.3 shows the response surface model contour plots of Idsat, Cgd and

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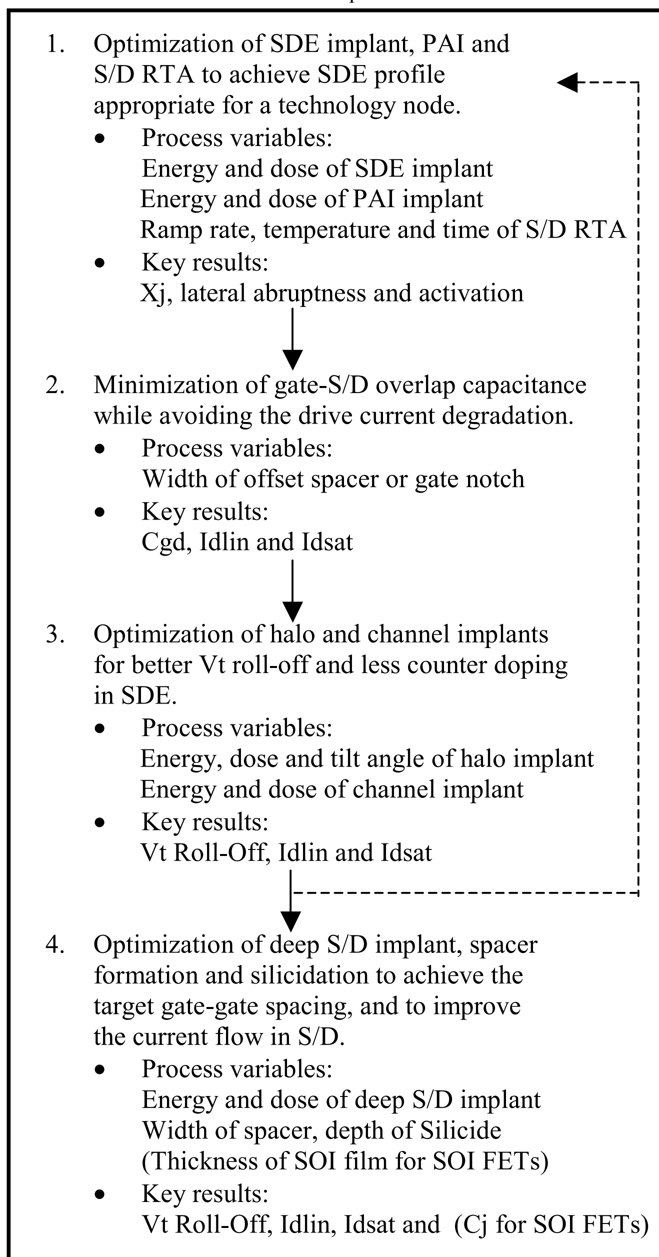
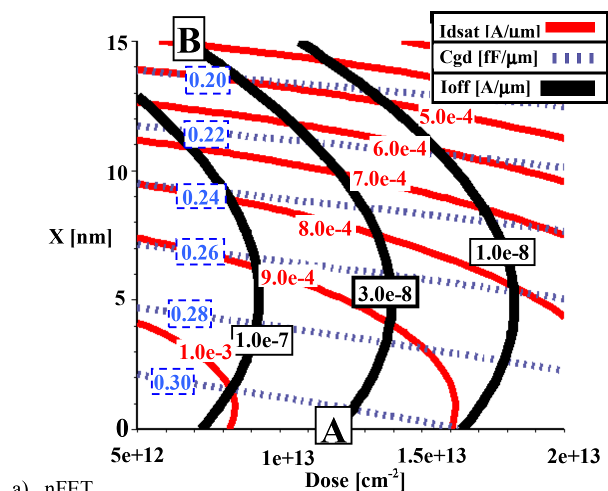
Ioff versus depth of Si recess (due to gate stack formation (X in Fig.1)) and channel implant dose for 40nm gate nFET and pFET. These plots indicate that increasing Si recess depth harms the FETs drive current. The off-current (Ioff, Vd=1.0V, Vg=0V) initially increases with increasing Si recess depth since the SDE implant into the deeper recess causes the deeper SDE junction. However, as the Si recess depth increases beyond ~5nm, Ioff starts to decrease. The saturation drive current (Idsat, Vd=Vg=1.0V) of nFET / pFET degrades by 57% / 53% with increasing recess depth following a constant Ioff=3.0e-8A/um from point A (0nm) to point B (15nm), respectively. The gate-S/D overlap capacitance (Cgd) of nFET / pFET is reduced by up to 37% / 36% with increasing recess depth given Ioff.

Table. 1: Transistor Optimization Scheme

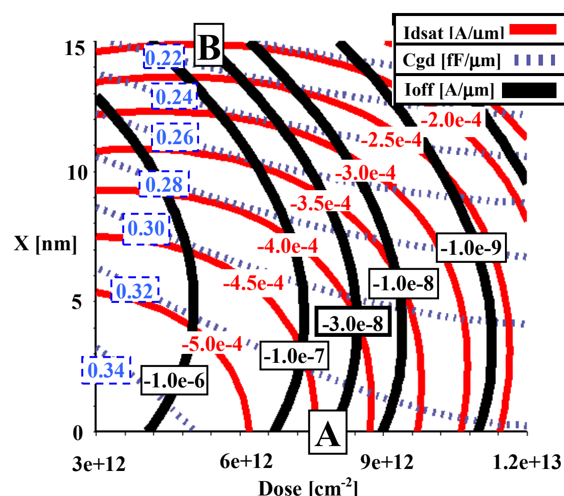


1. Optimization of SDE implant, PAI and S/D RTA to achieve SDE profile appropriate for a technology node.
   - Process variables:
     Energy and dose of SDE implant
     Energy and dose of PAI implant
     Ramp rate, temperature and time of S/D RTA
   - Key results:
     Xj, lateral abruptness and activation
2. Minimization of gate-S/D overlap capacitance while avoiding the drive current degradation.
   - Process variables:
     Width of offset spacer or gate notch
   - Key results:
     Cgd, Idlin and Idsat
3. Optimization of halo and channel implants for better Vt roll-off and less counter doping in SDE.
   - Process variables:
     Energy, dose and tilt angle of halo implant
     Energy and dose of channel implant
   - Key results:
     Vt Roll-Off, Idlin and Idsat
4. Optimization of deep S/D implant, spacer formation and silicidation to achieve the target gate-gate spacing, and to improve the current flow in S/D.
   - Process variables:
     Energy and dose of deep S/D implant
     Width of spacer, depth of Silicide
     (Thickness of SOI film for SOI FETs)
   - Key results:
     Vt Roll-Off, Idlin, Idsat and (Cj for SOI FETs)

Fig.4 shows that the silicon recess after SDE implant more severely degrades the FETs drive current than the silicon recess before SDE implant since the former removes some of as-implanted impurity from SDE region.



a) nFET



b) pFET

Fig. 3: Contour plot of simulated Idsat, Cgd and Ioff versus depth of Si recess due to gate stack formation (X in Fig. 1) and channel does of 40nm gate bulk FETs. Vdd=1.0V. Tgox=1.4nm.

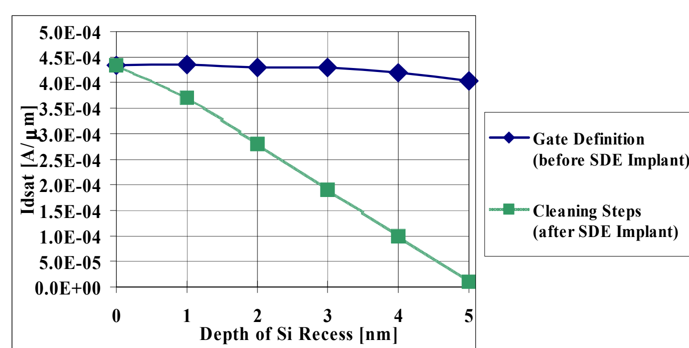


Fig. 4: Idsat versus depth of Si recess due to gate stack formation (before SDE implant) / cleaning steps (after SDE implant) of 40nm gate bulk pFET. Vdd=1.0V. Tgox=1.4nm. Both halo and channel implant dose are kept constant.

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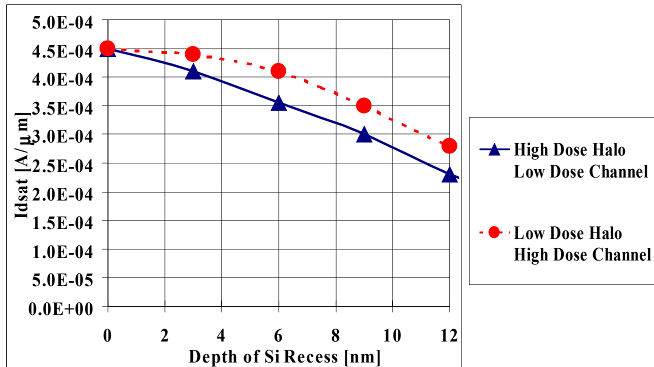
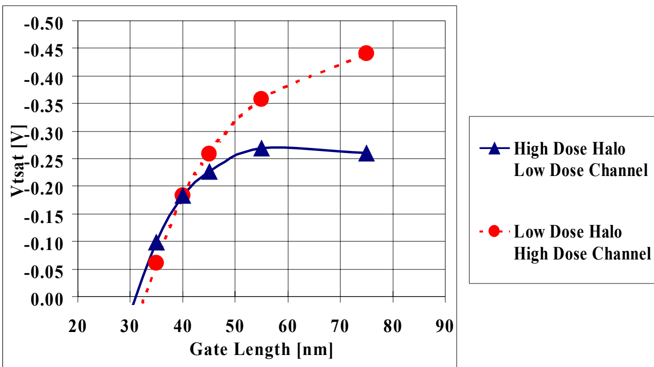
IV. OPTIMIZATION OF HALO

We optimize the halo and channel implants to achieve better Vt roll-off and less halo counter doping in SDE. In order to improve the FET performance and to mitigate the drive current degradation due to silicon recess, the net active doping concentration in the SDE should be maximized while maintaining a shallow junction. The optimization of S/D RTA condition effectively allows fabrication of an abrupt and highly activated SDE profiles. We found that the optimization of the pch halo implant condition can also help increase the pch SDE active doping concentration and improve the pFET performance by minimizing counter doping, especially in the lower-doped overlap region. Fig.5 shows the simulation of Idsat versus depth of silicon recess due to gate stack formation and the saturation threshold voltage (Vtsat) versus the gate length (Lg) for different halo dose. Ioff of 40nm gate pFET is adjusted to 30nA/µm by tuning channel dose. There is a trade-off. Increasing the dose of halo implant improves the short channel behavior but degrades the drive current of pFET. Fig.6 clearly indicates that using the steep halo helps increase the net active doping in pch SDE by suppressing halo counter doping in SDE area. Fig.7 shows the simulation of Ioff versus Idsat for different halo steepness. The steep halo (C) gives higher linear drive current (Idlin) and saturation drive current (Idsat) than the medium steep halo (B) by 8.2% and 6.4% and than the gradual halo (A) by 15.8% and 10.7%, respectively.

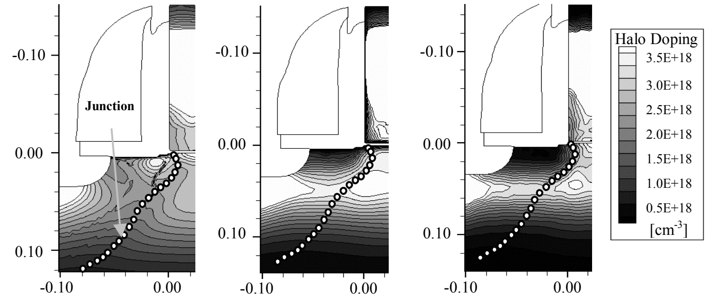


a)



b)

Fig. 5: Idsat versus depth of Si recess due to gate stack formation (a) and Vtsat versus Lg (b) for different halo dose of 40nm gate bulk pFET. Ioff of 40nm pFET is adjusted to 30nA/µm by tuning channel dose. Vdd=1.0V. Tgox=1.4nm.



a) Halo A (Gradual) b) Halo B (Medium) c) Halo C (Steep)

Fig. 6: Simulated 2D impurity doping concentration to compare pch halo steepness.

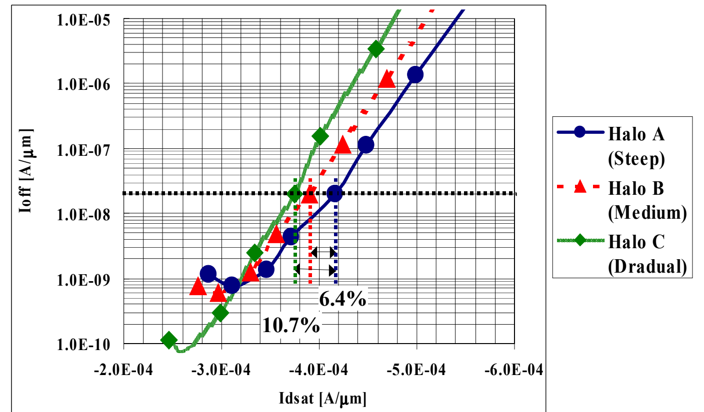


Fig. 7: Ioff versus Idsat of bulk pFET for different halo steepness. Ioff of 50nm pFET is adjusted to 20nA/µm by tuning halo dose. Cgd of 50nm device is 0.29fF/µm. Vdd=1.2V. Tgox=1.6nm.

V. OPTIMIZATION OF DEEP S/D, SPACER AND SILICIDE

Finally, we discuss the optimization of deep S/D, spacer width and silicide thickness to achieve the target gate-gate spacing while maintaining acceptable short channel margin, and to reduce the series resistance of the doping neck between SDE and deep S/D (Fig.2 a). The current flow beneath silicide is especially important for thin film SOI FETs (Fig.2 b). Fig.8 shows the contour plot of Idsat, Cgd and Ioff versus depth of Si recess due to spacer formation (Z in Fig.1) and channel implant dose for 40nm gate SOI nFET with SOI film thickness (Tsoi) = 50nm. Idsat degrades by 8% with increasing recess depth due to spacer formation following a constant Ioff=3.0e-8A/um from point C (0nm) to point D (15nm). This is because the Si-silicide interfaces move down with increasing the Si recess depth. Increasing the dose of deep S/D implant or the thermal budget of S/D RTA can get rid of the S/D doping neck but degrades the short channel behavior when the spacer width are minimized to archive the target gate-gate spacing and to reduce the series resistance in S/D. The FETs performance can be harmlessly recovered by reducing the silicon consumption due to silicidation (Fig.9). Using the raised S/D allows us to elevate the Si-silicide interfaces above the initial silicon surface, and significantly improves the performance of thin film SOI FETs (Fig.10).

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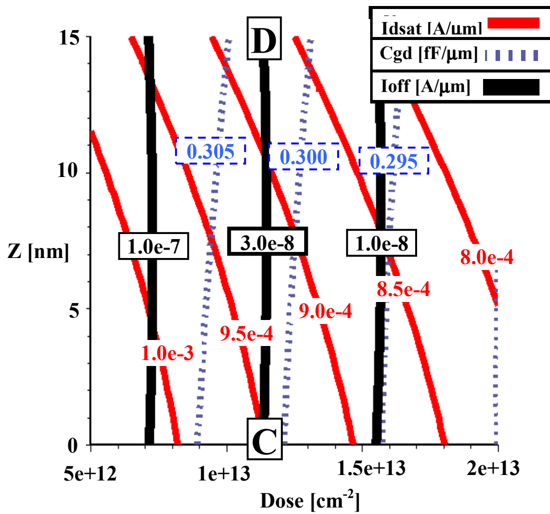
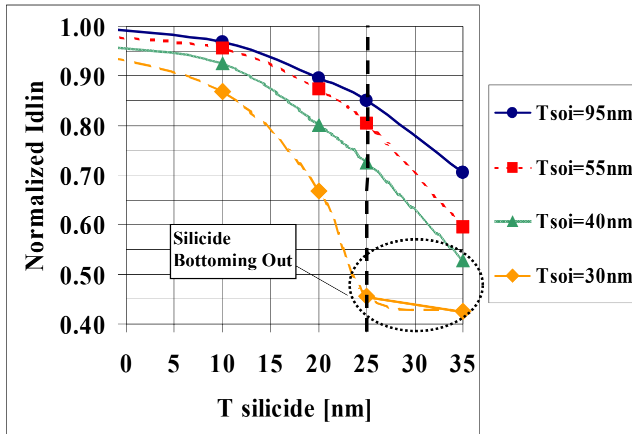
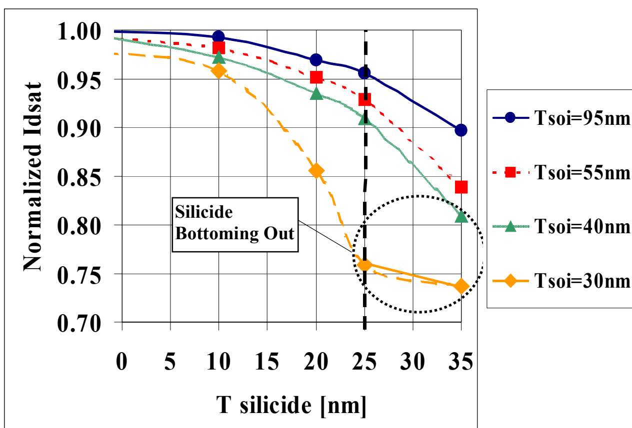


Fig. 8: Contour plot of simulated Idsat, Cgd and Ioff versus depth of Si recess due to spacer formation (Z in Fig.1d) and channel does of 40nm gate SOI nFET with Tsoi=50nm. Vdd=1.0V. Tgox=1.4nm.



a)



b)

Fig. 9: Normalized Idlin (a), Idsat (b) versus silicide thickness of 50nm gate SOI nFET for different SOI film thickness. The depth of Si recess (Z in Fig.1d) is 5nm.

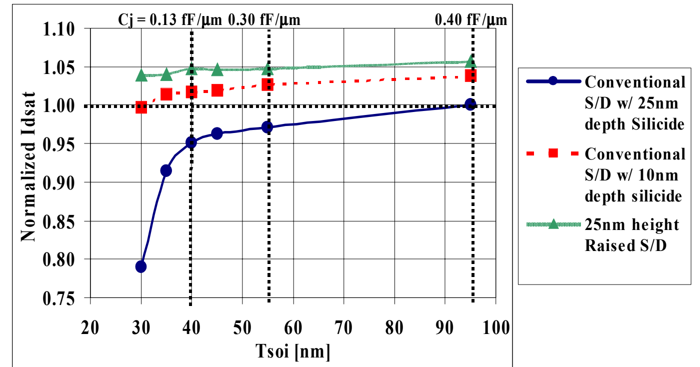


Fig. 10: Idsat versus Tsoi of 50nm gate SOI nFET for different silicide engineering. The depth of Si recess (Z in Fig.1d) is 5nm.

VI. SUMMARY

For a high performance sub-50nm MOSFET, the gate-S/D overlap distance should be minimized while avoiding significant increase of series resistance at SDE overlap region in order to improve the short channel margin, and to reduce gate-S/D overlap capacitance. The transistor characteristics become very sensitive to the depth of silicon surface gouging when the gate-S/D overlap distance is minimized. This study quantifies the sensitivity of the electrical characteristics of sub-50nm MOSFETs to the shape of silicon recess over S/D region due to over-etching during processing. It should be concluded, from what has been said above, that the silicon recess due to over-etching must be kept at a minimum for high performance MOSFET applications. Careful tuning of S/D, halo and silicide engineering is required to mitigate the drive current degradation due to silicon recess in S/D. Optimal ratio of channel to halo implant dose, steep halo, thinning silicide depth and using raised S/D improve the immunity of sub-50nm gate high performance MOSFETs to silicon recess problems.

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