A FinFET Design Based on Three-Dimensional Process and Device Simulations

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***Abstract*—In this paper, a practical design method of a FinFET is presented with an example of a scaled DRAM device. The electric properties of the FinFET are analyzed by means of three-dimensional process and device simulations. The analysis reveals that the short channel effects depend strongly on not only the thickness but also the taper angle of the silicon pillar. The device is optimized successfully assuming the tapered shape for the silicon pillar. The simulated characteristics (0.1fA off-leak current and 62μA drive current per unit cell @ 85C) well agree with experimental results.**

***keywords*—FinFET, DRAM, short channel effect, process simulation, device simulation, 3D**

I. INTRODUCTION

The FinFET is one of the promised candidates for post-planar devices because of its excellent roll-off characteristics, drive current and manufacturability [1]-[4]. The double gate structure makes it possible to overcome the short channel effects (SCE) with a lightly doped channel that yields low off-leak current (Ioff) and high drive current (Ion) simultaneously. This feature is advantageous for scaled devices especially of DRAM cells. However, an application of the FinFET to the scaled DRAM device is not an easy task since requirements for the extremely low Ioff (generally 0.1fA/cell @ 85C) complicates the design of the device. A key to success lies in the quantitative analysis of the SCE. The SCE of the FinFET are essentially three-dimensional phenomena that are sensitive to the geometry of the device. Therefore, three-dimensional process and device simulations are indispensable to design the FinFET with a short turn around time.

Using fully three-dimensional process and device simulators: HySyProS and HyDeLEOS [5], we have successfully designed a FinFET for an 110nm DRAM device. In Fig.1, a schematic of the target DRAM device is illustrated. The FinFET consists of the pillar-shaped active area and the fin-shaped buried gate, which operates as a transfer gate between the storage node and the bit-line. The active area is connected to the substrate electrically in order to discharge majority carriers and prevent a fatal transition of the threshold voltage. The thick pad-nitride isolates the active area from the top-gate. The specification of the FinFET is listed in Table I. The upper limits of the dopant concentration are empirically determined to restrain the extra leakage from the band-to-band tunneling. For achieving the aggressive Ion/Ioff, the shape of the silicon pillar is optimized with a dedicated consideration to the geometrical effect of the SCE following a selection of the gate-material. Finally, the predicted characteristics are compared with experimental results.

TABLE I. SPECIFICATION OF FINFET

Parameter	Value
Nominal Gate Length	110nm
Channel Region Height	150nm
Gate Oxide Thickness	5nm
Off-Leak Current (extrapolated)	0.1fA/cell
Drive Current	50μA /cell
Channel Dopant Concentration	$\leq 2\times10^{17}cm^{-3}$
Source/Drain Dopant Concentration	$\leq 2\times10^{18}cm^{-3}$

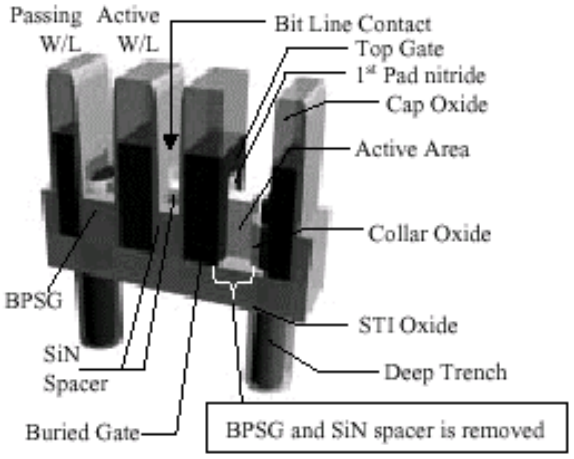

Figure 1. A schematic of the target DRAM device. It includes two unit cells that share the bit-line contact. The FinFET consists of the pillar-shaped active area and the fin-shaped buried gate, which operates as a transfer gate.

II. SIMULATION BASED DESIGN

A. Selection of the Gate Material

Solving a simplified one-dimensional Poisson's equation derives an expression for the threshold voltage of the FinFET as follows:

$$V_{TH} = \Delta\Phi + 2\varphi_F + \frac{qN_{CH}}{C_{OX}}\left(\frac{T_{CH}}{2}\right)$$

where $\Delta\Phi$ means a difference in the fermi levels of the channel and the gate-material. The symbols φ_F, C_{OX}, N_{CH} and T_{CH} represent the fermi potential, the gate-capacitance per unit area, the channel dopant concentration and the channel thickness (or the pillar thickness), respectively. The second and the third terms are negligible for scaled devices with lightly doped thin channel regions. Hence, a selection of the gate-material is an important task to adjust the threshold voltage. For our target device, the p-type polycrystalline silicon is suitable as a gate-material, with which the threshold voltage comes to approximately 1 volt. Particular processing techniques would be required because the p-type polycrystalline silicon often causes a crucial fluctuation of the threshold voltage due to the dopant diffusion into the channel.

B. Analysis of the Short Channel Effect

The channel thickness is an essential factor for controlling the SCE of the FinFET. A thin channel enhances the controllability of the gate electrode, consequently the punch-through current decreases. The dependency of the Ioff on the channel thickness is analyzed through systematic simulations assuming ideal block-shaped structure and typical processing conditions to estimate the channel thickness required for the Ioff of 0.1fA. In Fig.2, the estimated channel thickness is given as a function of the gate-length and the gate-oxide thickness. It can be seen that a channel thickness of 80nm with T_{OX} of 8nm or 100nm with T_{OX} of 3nm is required when the gate-length equals to 110nm. The worst-case value of 80nm is adopted as the target channel thickness since the gate-oxide thickness tends to be thicker than the target value of 5nm due to an intensive post-oxidation process.

At the bottom of the silicon pillar near the substrate, the dopant profile has a much influence on the punch-through current because the controllability of the gate electrode diminishes there. In Fig.3, an optimized well profile is shown. The locally high dopant concentration near the substrate contributes to the reduction of the punch-through current and the leakage from the band-to-band tunneling simultaneously.

The shape of the silicon pillar depends on the etching process of the substrate. We examined the geometrical effect on the electric properties of the FinFET with process and device simulations for three different shapes of the silicon pillars illustrated in Fig.4. The device structure and the dopant profile simulated by HySyProS for the tapered shape (C) are shown in Fig.5. The electron concentration calculated by HyDeLEOS is shown in Fig.6 and Fig.7. In Fig.8, the Ids-Vgs characteristics of the three devices are compared. It is found that the tapered shape gives lower Ioff and higher Ion than the ideal shapes (A) and (B). The increase of the Ion observed in the tapered shape is owing to the decrease of the parasitic resistance in the source and drain regions, namely, a larger number of impurity atoms is implanted into the source and drain regions. On the other hand, the decrease of the Ioff is ascribed to the suppression of the punch-through current in the top of the channel due to the thin channel thickness in that region. From Fig.6 and Fig.7, it is obvious that the high dopant concentration of the source and drain regions near the top of the channel induces a critical punch-through path which is defused by the tapered shape. The actual shape of the fabricated device corresponds to the tapered shape.

C. Analysis of the Mobility Degradation

We further investigated the effect of the mobility degradation that arises from the channel parallel to the (110) crystalline plane. The simulated and measured universal curves are compared in Fig.9 for (100) and (110) planes. The resultant Ids-Vgs characteristics are shown in Fig.10. Although a 20% reduction in the drain current is observed, the drive current is still sufficient even when the channel is parallel to the (110) plane.

D. Optimization of the dopant profiles

Finally, the processing conditions are optimized in detail performing the process and device simulations iteratively. The primal objective is an improvement of the Ion/Ioff by controlling the dopant profile of the source and drain regions. A simple fair diffusion model is applied here with intent to shorten the simulation time. However, the simulated dopant profiles are accurate since point defects do not contribute to the dopant diffusion in the narrow silicon pillar.

It should be noted that the fully calibrated parameters are used in the above-mentioned simulations.

III. RESULT

The predicted Ids-Vgs curves are shown in Fig.11 with the substrate biases of 0V and –0.5V. The Ion/Ioff of 62μA/0.1fA is observed. It is also found that the substrate bias effect is negligible due to the fully depleted operation of the device. This feature is preferable for high performance DRAM devices.

In Fig.12, the measured Ids-Vgs curve is shown. The measured Ion/Ioff (32μA/1pA) is much smaller/larger than the simulated value. The large discrepancies are owing to the following two reasons. One is a large parasitic resistance. The other is a large flat-band shift that might be derived from the fixed charge and the interfacial states. Taking into account of these effects, we performed an additional simulation whose result is included in Fig.11. The simulated Ion/Ioff (28μA/0.5pA) well agrees with the experimental result. This fact reveals that we can achieve target Ion/Ioff by reduction of the parasitic resistance and the flat-band shift.

IV. CONCLUSION

We have presented an application of three dimensional process and device simulations to a design of the FinFET for the 110nm DRAM device. The comparison with experiment demonstrates the validity of the design and its method.

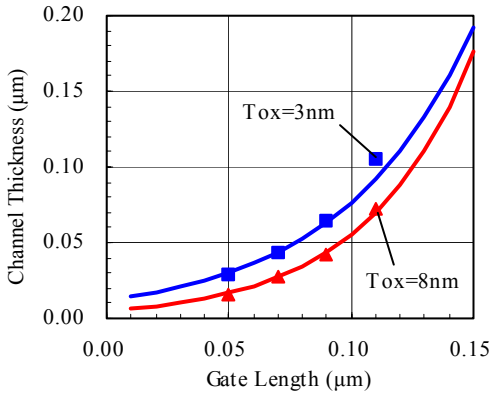

Figure 2. The channel thickness required for the off-leak current of 0.1fA. The square and the triangular symbols represent simulated results for the gate oxide thickness of 3nm and 8nm, respectively.

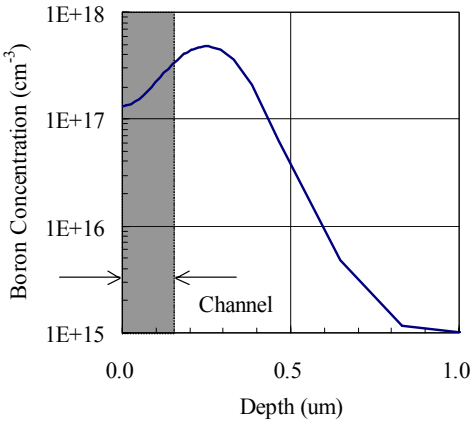

Figure 3. The optimized well profile simulated by HySyProS. The top and the bottom of the silicon pillar are located at the depth of 0μm and 0.25μm, respectively.

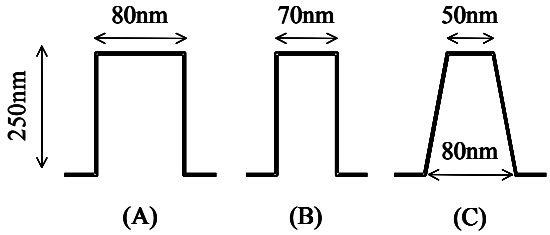

Figure 4. A schematic illustration of a cross-section of the silicon pillar. Two ideal block-shaped pillars with different thicknesses (A) (B) and a taper-shaped pillar (C) are examined. The initially estimated shape is (A), meanwhile, the actual shape of the fabricated device is (C).

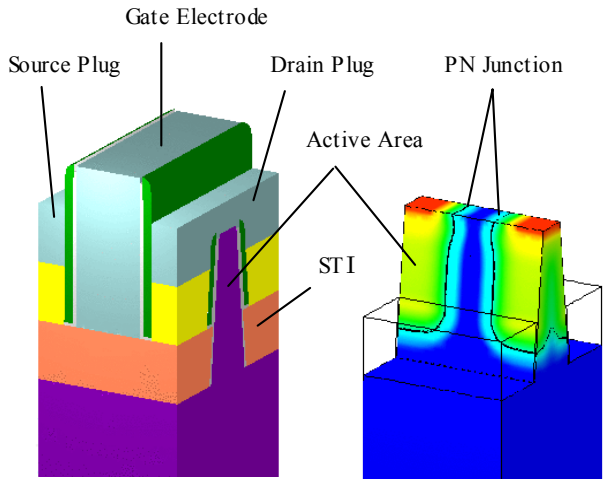

Figure 5. The device structure (left-side) and the dopant profile (right-side) simulated by HySyProS for the tapered shape (C) in Fig.4. Total number of grids is 105,748 in this case. Note that the polygonal mesh is used for incorporating the tapered-shape efficiently and accurately.

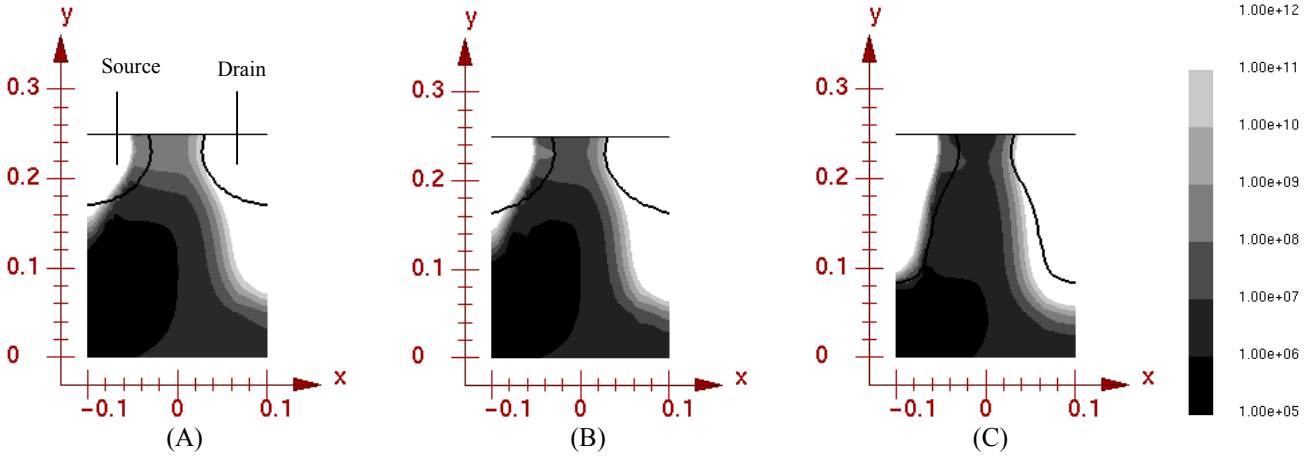

Figure 6. Simulated 2-D electron concentration at the off state on a cross-section at the middle of the silicon pillar for each shape in Fig.4. The solid lines in the source and drain regions indicate the metallurgical PN-junctions.

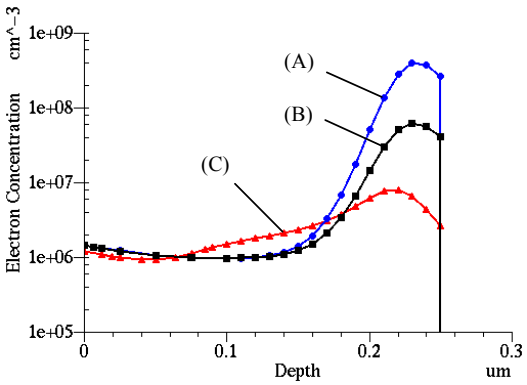

Figure 7. Simulated 1-D electron concentration at x=0 (center of the channel) of each crosssection in Fig.6. With the tapered shape (C), the punch-through current near the top of the channel decreases.

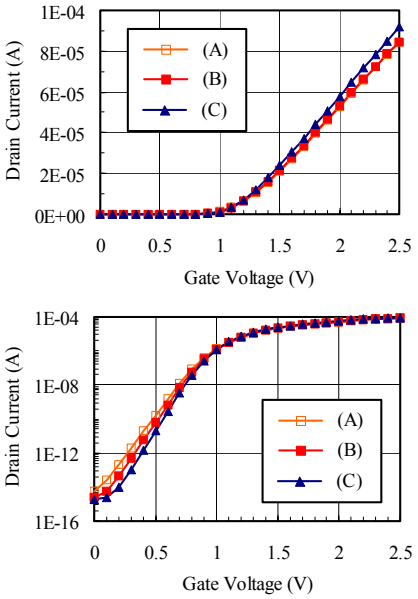

Figure 8. Simulated Ids-Vgs characteristics for the three different shapes of the silicon pillars in Fig.4. The tapered-shape (C) gives higher drive current and lower off-leak current than others.

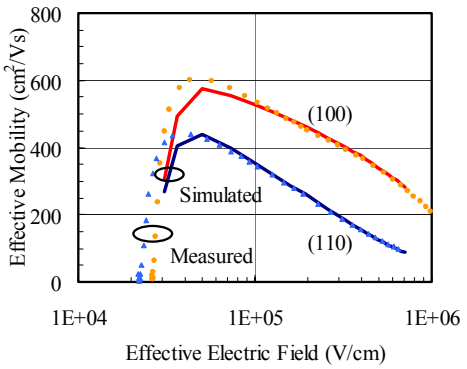

Figure 9. Measured (marks) and simulated (lines) universal curves for (100) and (110) crystalline planes at the temperature of 347K.

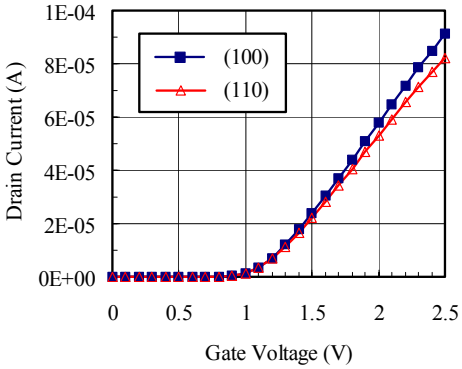

Figure 10. Simulated Ids-Vgs characteristics with (100) and (110) mobility models.

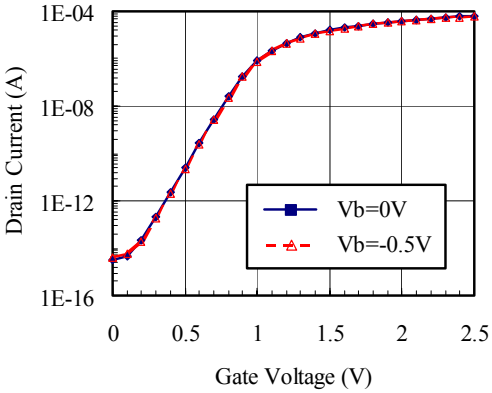

Figure 11. Simulated Ids-Vgs characteristics after the optimization of the dopant profiles. The contact resistances of the source and drain plugs are included in the simulation.

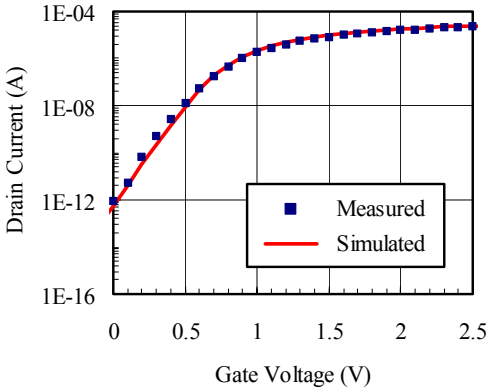

Figure 12. Measured and simulated Ids-Vgs characteristics of the fabricated device.

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