Electrostatic Analysis of Carbon Nanotube Arrays

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***Abstract*—In order to improve the performance of carbon nanotube field effect transistors (CNFETs), a nanotube array should be used. For a densely packed array of nanotubes, screening by nearby tubes affects the capacitance per tube. The gate-to-channel capacitance for a nanotube array of three different gate electrode configurations was examined in this study. Simulation results show that a wrap-around gate gives the largest gate-to-channel capacitance among the three gate configurations. A bottom gate structure, in which carbon nanotubes are unpassivated, presents a distinct electrostatic disadvantage of the weakest gate control. For a top gate structure, we found that an optimum design point exists for the *pitch*, which is defined as the distance between the centers of adjacent nanotubes, to get the largest gate capacitance per unit area.**

Keywords: carbon nanotube, field effect transistor, CNFET, nanotube array, gate configuration, gate capacitance, screening effect.

I. INTRODUCTION

Silicon based MOSFET technology will eventually reach its limit. In order to continue improving the density and performance of electronic products, new integrated circuit technologies are explored. Carbon nanotubes are among the promising candidates in future electronic systems [1,2,3]. CNFETs have been reported and they may be competitive with Si FETs in the sub-20nm gate length regime [4,5,6,7,8]. Many early CNFETs reported used a planar bottom-gate electrode configuration, in which the carbon nanotube is unpassivated [3,4,7]. In this design, the thickness of the back gate dielectric is usually around 100nm or more. Due to the lower dielectric constant of the air surrounding the carbon nanotube and larger thickness of the gate dielectric, the gate-to-nanotube capacitance is small, which implies lower on-current. For the top-gate geometry, the carbon nanotube is covered by a gate insulator, which offers advantages over the bottom-gate design [5,6,8], such as lower operating voltage due to stronger coupling between the gate and the nanotube and more flexibility to control individual devices. Another possible gate design for CNFETs is a wrap-around gate [7], in which the carbon nanotube is surrounded by a cylindrical gate. This coaxial structure exhibits the strongest capacitive coupling between the gate and the tube.

Since a single nanotube provides little current drive, in order for CNFETs to deliver current for driving long capacitive interconnect wires, an array of carbon nanotubes would be required. By analogy with silicon MOSFETs where on-current is proportional to the charge induced by the gate, we consider channel charge per unit length $Q_L=C_L(Vg-Vt)$, where C_L is the gate-to-channel capacitance per unit length. This on-current relationship only applies to CNFETs with an ohmic contact. Nevertheless, even for the case of a source/drain with a Schottky contact [9], understanding the gate capacitance of CNFETs will also help benchmark device performance against conventional silicon devices [10] since the gate capacitance is the load capacitance for the preceding logic stage. In addition, it is crucial to take a closer look at the gate-to-channel capacitance for CNFETs formed from an array of nanotubes. When the nanotube array becomes more densely packed the screening effect of nearby tubes is important.

II. DEVICE MODLEING

Three different gate electrode configurations (a conformal top-gate, a planar bottom-gate only and a fully surrounding wrap-around-gate) for CNFETs are considered here as shown

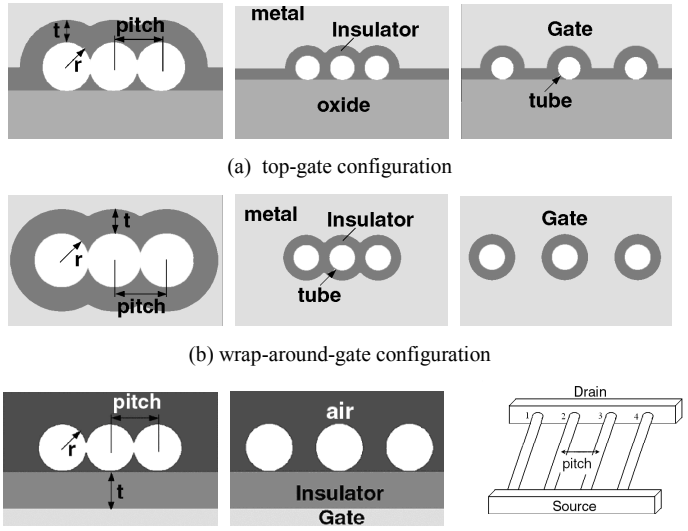

Figure 1. Three different gate electrode configurations for CNFETs.

in Fig.1(a,b,c). Each nanotube in an array has identical radius r (r = 0.7 nm or r = 1.5 nm). The gate dielectric is assumed to be SiO_2 (κ= 3.9) with thickness t. Identical nanotubes are placed in an array with uniform spacing. *Pitch* is defined as the distance between centers of adjacent nanotubes (see Fig. 1(d)). When neighboring nanotubes just touch to each other, we define the minimum *pitch* value $pitch_0 = 2r$. By varying *pitch,* we obtain different images as shown in Fig. 1 (a, b, c). In this

work, numerical solutions are obtained by solving the 2D electrostatics of the nanotube array. The gate-to-channel capacitance for a nanotube array is analyzed for different *pitch* and *t/r* ratios since the capacitance depends on *t/r* ratio rather than *t* or *r* alone. FIELDAY [11] was used to perform the device simulations and capacitance information was obtained by small-signal A.C. analysis [12]. Throughout the simulations, the nanotube is treated as a classical metal with equal potential over the tube [13]. We do this in order to simplify the problem and focus on the question of interest: how screening by nearby tubes affects gate-to-channel capacitance. Note that the gate capacitance C_L is the series combination of the insulator and quantum capacitance. In order to obtain more accurate results, quantum capacitance should be included in the simulations. However we have not done this, so our simulation results slightly overestimate C_L. Our results still indicate the general trends to be expected for the gate to channel capacitance of nanotube arrays over a range of packing densities.

III. SIMULATION RESULTS AND DISCUSSION

We assume all middle tubes in an array, with right and left neighbors, have the same gate-to-tube capacitance. In Fig. 2,

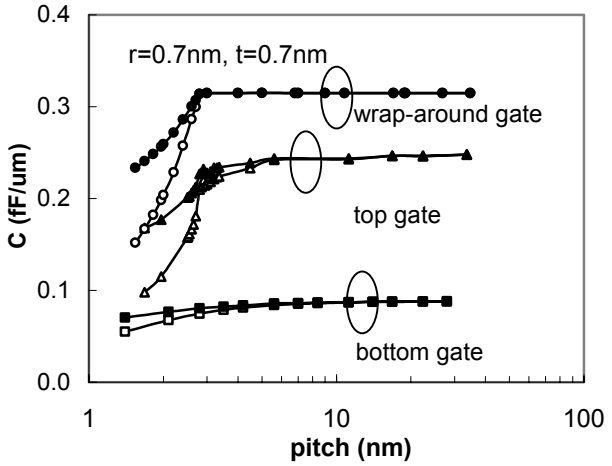

Figure 2. The gate-to-end-tube capacitance (solid symbols) and the gate-to-middle-tube capacitance (open symbols) vs. pitch for three gate configurations.

we compare the gate-to-end-tube capacitance (solid symbols) with the gate-to-middle-tube capacitance (open symbols) for three gate configurations. We can see that the tubes at the end of an array have higher capacitance than that of the middle tubes when they are closely packed (*pitch* is small). This is because end tubes have larger arc coupling to the gate electrode. For the bottom-gate structure, this difference is small, because in that configuration, the electrode does not wrap around the end tubes. Fig. 2 also shows that there is significant advantage for a wrap-around-gate structure. We can expect an increase in capacitance by 30%-50% compared to the top-gate configuration, and an increase by a factor of 2~3 compared to the bottom-gate configuration.

Among the three gate electrode designs, the top-gate structure shows several advantages over the bottom-gate

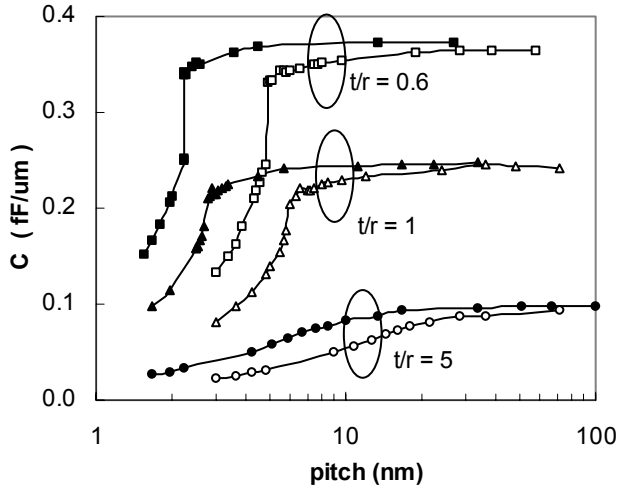

Figure 3. The gate-to-middle-nanotube capacitance vs. pitch for the top-gate configuration. Solid symbols are for r=0.7nm and open symbols are for r=1.5nm.

structure [6] and is easier to fabricate than the wrap-around-gate. In Fig. 3, we vary the *t/r* ratio and the radius *r* of the nanotube for the top-gate configuration. It shows that a smaller

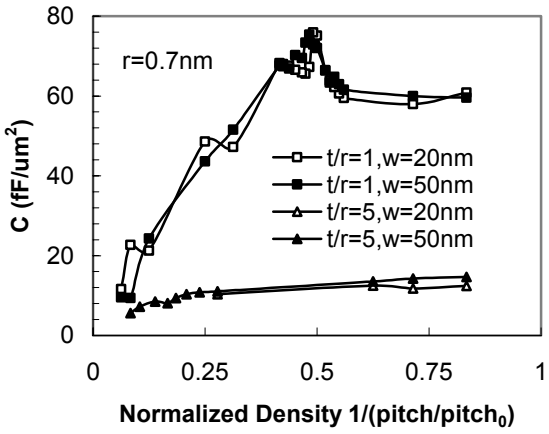

Figure 4. The gate-to-nanotube capacitance per unit area vs. normalized density for the top-gate configuration (pitch$_0$=2r).

t/r ratio gives a larger capacitance due to the thinner gate dielectric and a larger relative gate coupling area. Note that when the *t/r* ratio is small (*e.g. t/r*=0.6) and $2r < pitch \le 2(t+r)$, capacitance increases as *pitch* increases. There is an abrupt change when *pitch* is just above *2(t+r)* due to more metal wrapping around the dielectric, achieving more coupling between the gate and the nanotube. After this critical point, the capacitance curve becomes more nearly flat.

Considering the difference in capacitance between end and middle tubes shown in Fig. 2, we estimate the capacitance per unit layout area for a multi-tube array as

$$C = [(n-2)\times C_{middle} + 2\times C_{end}] / w, \quad (1)$$

where n is the total number of tubes in the array, w is the device width, and C_{middle} and C_{end} are the gate-to-middle-tube and the gate-to-end-tube capacitance respectively. Fig. 4 shows the capacitance per unit layout area versus reciprocal pitch for different w. Irregularity of the curve results from our allowing only an integral number of tubes to rest on a given layout area. For the top-gate structure, we found that when the t/r ratio is small (*e.g.* smaller than 2), an optimum point exists to obtain the largest capacitance per unit layout area, where *pitch* is just slightly larger than $2(t+r)$. In Fig. 4, in the region of $pitch > 2(t+r)$, left of the peak, capacitance per unit area decreases as fewer nanotubes occupy the same area. In the region of $2r < pitch < 2(t+r)$, right of the peak, the case becomes more complex. Figures 5a and b compare two CNFET arrays, differentiated by their *pitch*. For Fig. 5a, $pitch \le 2(t+r)$, while for Fig. 5b, $pitch > 2(t+r)$. We assume that the dielectric is deposited non-selectively, and we assume an idealized conformal shape for the dielectric layer, such that the relation $h > t$ is satisfied in Fig. 5a, and $h = t$ in Fig. 5b, including complete under-filling. From Fig. 5a, we estimate the gate capacitance per unit area (neglecting an end-tube correction) by

$$\overline{C} = C_0 \times \{2\times(t+r)\times \arcsin[0.5\times pitch/(t+r)]/pitch\}$$
$$= C_0 \times \left\{(\frac{t}{r}+1)\times\frac{pitch_0}{pitch}\times\arcsin\left[\left((\frac{t}{r}+1)\times\frac{pitch_0}{pitch}\right)^{-1}\right]\right\} \quad (2)$$

where

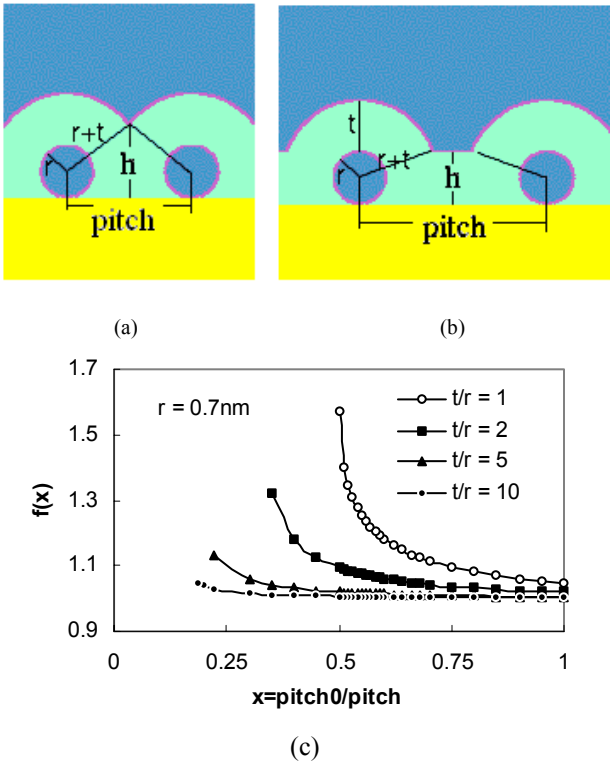

Figure 5. For the top-gate structure (a) the case that the top arc length of each tube increases as pitch increases; (b) the case that the top arc length of each tube does not change as pitch increases; (c) f (x) vs. x.

$$pitch \le 2(t+r) \quad \Rightarrow \quad pitch_0/pitch \ge 1/(1+t/r).$$
$$h \ge t \quad \Rightarrow \quad pitch_0/pitch \ge 1/(2\sqrt{t/r}) \quad (3)$$

C_o represents a capacitance per arc length and is a function of t, r, and κ; and $f(t, r, pitch)$ is defined by the quantity in braces. In Fig. 5c, we plot $f(x)$ vs. $x=pitch_0/pitch$ for different t/r ratios. The curves are constrained on the right by the criterion of $pitch \ge pitch_0$, and on the left by the $h \ge t$ criterion. We found that when t/r ratio is small, $f(x)$ greatly decreases as tubes are more closely packed (normalized density, $pitch_0/pitch$, increases). In the case of $r=t=0.7nm$, the top curve in Fig. 5c can be compared to the right half of the

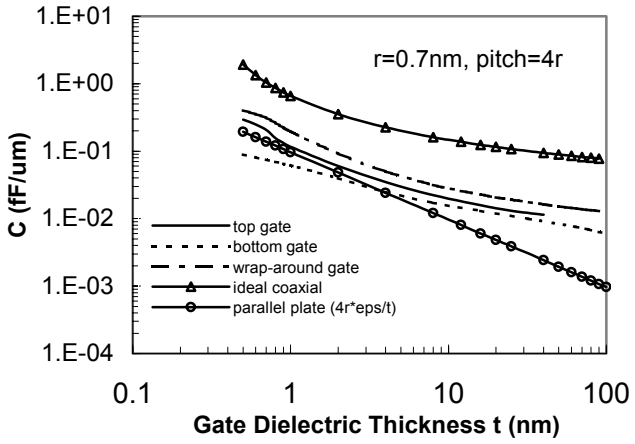

Figure. 6 Capacitance vs. t for three gate configurations and compare that to the case of the MOSFET, which is parallel plate

corresponding curve in Fig. 4.

For Fig. 5b, Eq. 2 no longer holds. In this case, as t is increased, C_o would decrease, and the arc length increase is dependent on h (=t) *vs.* r, with a further, weak component

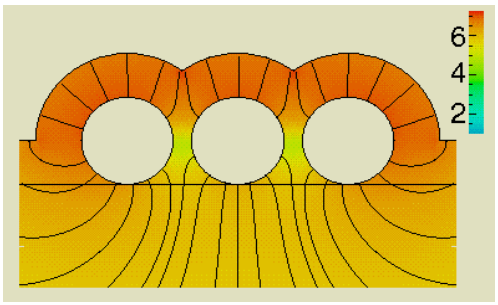

Figure 7. Black lines show electric field directions and the color map shows the magnitude of electric field (unit: V/cm with log scale) for the top gate configuration with r = 0.7nm, t = 0.7nm, pitch = 1.68nm.

from the flat region seen in the Fig. 5b. Since fewer nanotubes occupy the given area as *pitch* increases, the capacitance per unit layout area decreases, in a manner similar to that of a bottom-gated CNFET array [13].

Fig. 6 shows capacitance versus t for a fixed r (=0.7 nm) and a fixed *pitch* (= $4r$) for the three cases (top, bottom and wrap-around) and compares these to the case of a MOSFET, represented as a parallel plate capacitor with $C=d\kappa/t$ (assume

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$d=4r$ in order to compare with nanotube capacitance) and an ideal coaxial capacitor with $C=2\pi\kappa$ / ln (t/r+1). Here we include the screening effect of nearby tubes, and the capacitance of the wrap-around-gate configuration is lower by a factor 3~6 compared with previous simplified results [7] which represented the tube as an ideal coaxial capacitor without screening.

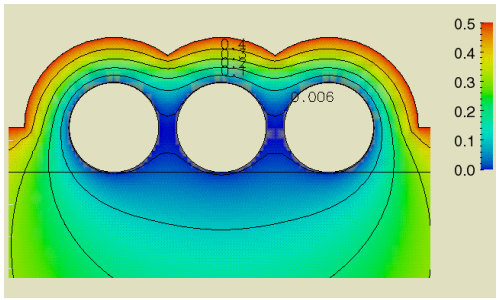

Figure 8. The electric potential contour for the top-gate configuration with r=0.7nm, t=0.7nm, pitch=1.68nm. Potential lines are at 0.1V increments.

In Fig. 7, black lines show electric field direction and color map shows the magnitude of electric field for the top-gate structure. We can see that on the top the nanotubes (top arc area), electric field is strong and the magnitude of the electric

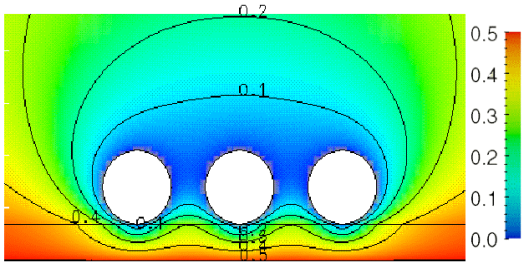

Figure 9. The electric potential contour for the bottom-gate configuration with r=0.7nm, t=0.7nm, pitch=2.1nm. Potential lines are at 0.1V increments.

field is uniform. Figs. 8~10 show the electric potential contours for the three gate configurations when we apply 0.5V to the gate electrode. From those plots, it is clear to see the screening

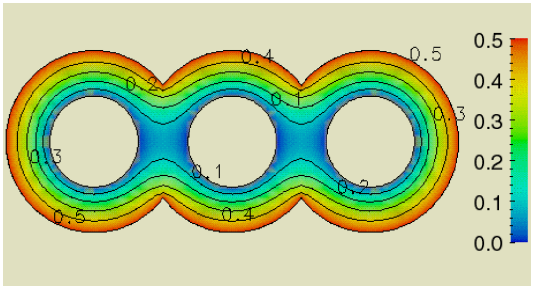

Figure 10. The electric potential contour for the wrap-around-gate configuration with r=0.7nm, t=0.7nm, pitch=2.2nm. Potential lines are at 0.1V increments.

and the fringing field.

IV. Conclusion

The gate-to-channel capacitance of three possible gate configurations for CNFETs has been studied. Due to the largest gate-to-channel capacitance among three designs, there is significant advantage for a wrap-around-gate over either a top-gate or bottom-gate configuration. However there is complexity of fabrication for the wrap-around-gate structure. A top-gate CNFET with a structure similar to that of conventional silicon MOSFET, is a better candidate compared to a bottom-gate CNFET. In order to improve current drive capability, a nanotube array would be used. Simulation results show that, for the top gate configuration, the distance between the neighboring tubes can be optimized to get the largest gate-to-channel capacitance per unit layout area for small t/r ratio cases, which implies higher on-current.

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