Simulation of surface engineering for ultra shallow junction formation of PMOS for the 90nm CMOS technology node and beyond

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Abstract—**Since the junctions in the most advanced CMOS devices are thinner and thinner, the influence of the surface of silicon is thus becoming significant on dopant diffusion. In this paper, based on experimental data, a methodology for calibration is proposed, taking this effect of surface into account. SIMS profiles are accurately fitted by simulation using a simple model of recombination of interstitials; the phenomenon of POED is well reproduced and validated by TCAD 1D simulations. Then, the impact of POED on the PMOS performances is quantified by anticipation with 2D TCAD simulations.**

Keywords- Boron; diffusion; interstitial recombination; POED; TCAD

I. INTRODUCTION

In advanced CMOS technologies (sub 0.1µm), ultra shallow junction (USJ) optimization is becoming a key issue for the development of advanced MOS device. According to [1], the targeted junction depth for the 90nm node is 30 nm in year 2004. On an other hand, as far as the junction depth is decreasing, the surface is more and more becoming critical for the control of dopant diffusion. A new effect has been shown in the litterature [2], the POED (Post Oxidation Enhanced Diffusion), dealing with the influence the of surface on transient diffusion of boron. The aim of this paper is to model this effect with a commercial simulation tool. In a first step, the simulator is calibrated. In a second step, the model is used to anticipate the impact of this effect on the device, in order to guide the development of the 90nm node.

II. EXPERIMENTAL

The experimental results are based on the work of D. Lenoble ([2]) who has highlighted the Post Oxidation Enhanced Diffusion. In this work, a 1.5nm thick oxide was grown on n-type,<100> CZ silicon wafers. Then, oxide was etched on half of the lot, and all samples were annealed with a standard RTA annealing at high temperature (1050°C, 10s) in order to recover the interstitials supersaturation induced by the oxidation, and to eliminate dislocation loops eventually formed during oxidation.

Then, the samples were implanted with boron at various energies (0.4, 3, 5, 10keV), with the same dose of 1e15cm^{-2} either through a thin sacrificial thermal oxide or through a bare surface (native oxide only) and analysed by SIMS to get boron depth profiles. As can be seen on figure 1, the lower the energy, the more the diffusion is enhanced by the presence of the thermal oxide. At 10keV, almost no difference is visible on SIMS profiles with and without oxide. The diffusion length is therefore dramatically increased with an oxide cap.
Complementary experiments were performed:
A) different kinds of cleaning were tested, leading to different qualities of native oxide: no difference was noticed after diffusion. As a conclusion, POED is not dependant of the stoechiometry of the oxide.
B) the thermal oxide thickness was varied (in such a range that the amount of dose in the oxide after implantation remained negligible): the same diffusion length was observed for all samples.
C) The sacrifical oxide was deposited by CVD: POED could not be suppressed.
Experiments B and C show that the interstitials injected during the thermal oxidation for SACOX are not responsible for POED.

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The assumptions proposed by [2] is that thermal oxide modifies the surface capability of trapping Si interstitials on recombination centers at the interface Si/SiO_2. As a result, the amount of defects is higher during the annealing when an oxide is present, increasing thus the POED of Boron.

The goal of this work was then to validate this assumption with TCAD simulations and to calibrate the simulator.

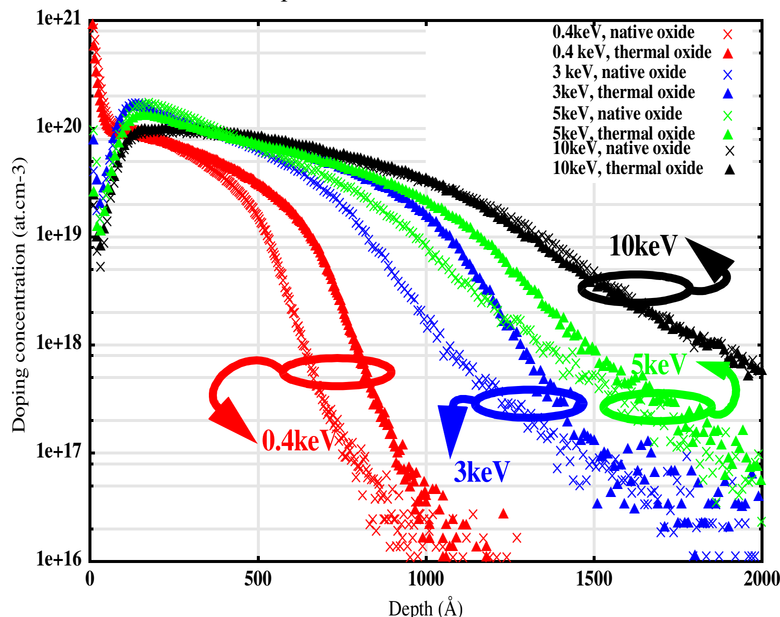

Figure 1. *SIMS profiles of boron after a 1050°C, 15s annealing, with or without thermal oxide capping*

III. MODEL DESCRIPTION

TCAD simulations were performed with the ISE^{TM} 6.1 tools package [3]. The modification of the surface recombination capability induced by a thermal oxide was modelled with the following reaction term:

$$\vec{j} \cdot \vec{n} = k \cdot (I[0] - I^*[0])$$

Where: n denotes the outer unit vector normal to the surface (Si/SiO2), j denotes a flux toward the interface, k stands for the recombination rate of interstitials at the interface Si/SiO2, I[0] is the interstitial concentration at 0nm, I*[0] is the equilibrium concentration at 0nm with respect to the interface.

The simulation strategy is described on figure 2 . We assumed a "+1" model ([4]) for damages after implantation, and a coupled pair-defect diffusion model ([5])). First, the profile is roughly fitted on the SIMS profiles done on samples with thermal oxide, the model of recombination at the interface being deactivated.

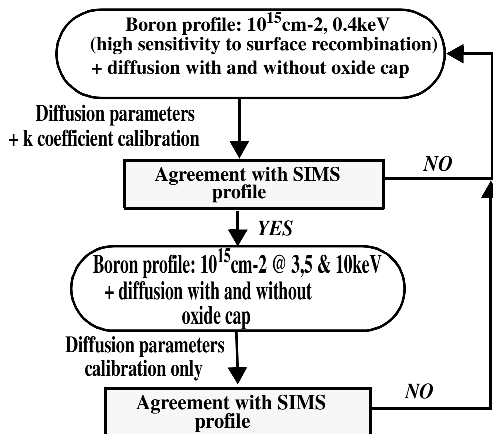

Figure 2. *Calibration strategy*

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Then, the recombination model was activated and the parameter k was fitted for a finer agreement of simulated profiles on SIMS data, after many iterations, both for a surface with a native oxide and with a thermal oxide. The energy of 0.4keV was chosen for the calibration because the effect of POED is the most important as it is the lowest energy.

Two values were fixed for the coefficient of recombination k, at a temperature of 1050°C: one for a native surface ($k1=5.0x10^7 s^{-1}$) and one for a thermal oxide ($k2=1.4x10^7 s^{-1}$). Simulations were then validated at 3keV, 5keV and 10keV with the same values for the parameter k as previously deduced: as can be seen on figure 3, the POED is quite accurately reproduced with the recombination model chosen, in the range of energies [0.4keV ; 10keV].

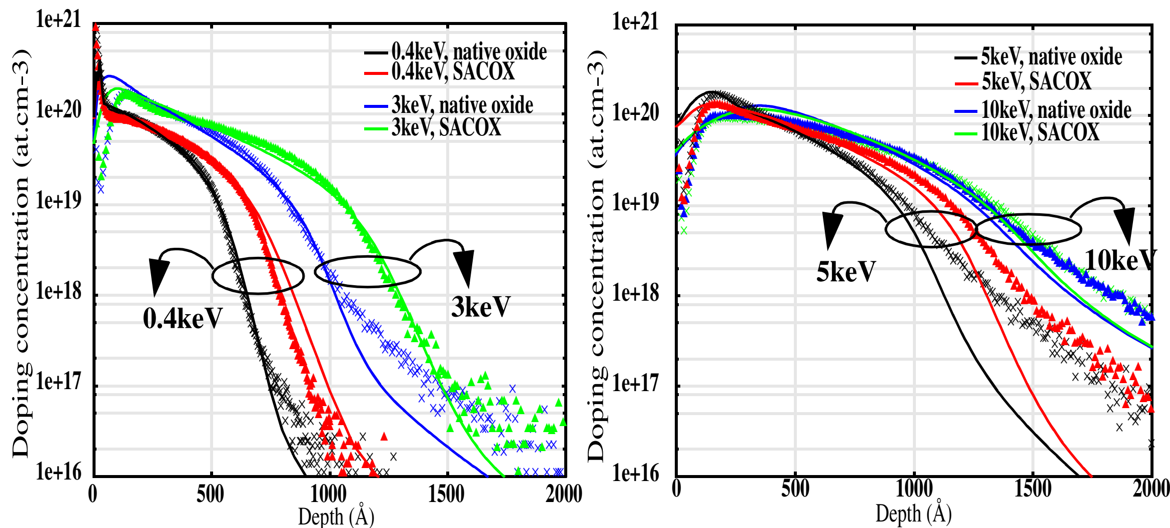

Figure 3. *POED effect, comparison between simulated profiles and SIMS (dotted lines: SIMS, solid lines: simulation)*

The evolution of the simulated profile for interstitial as a function of the time of annealing is shown on figure 4, without oxide and with thermal oxide. The hypothesis of [2] seems to be verified: a native oxide is porous, many bounds are dangling; as a result, the surface acts as a sink for interstitials and decreases their concentration beneath the interface, the TED is thus lessened. With a thermal oxide, almost stoechiometric, less recombination of interstitials is possible at the interface: TED is more important.

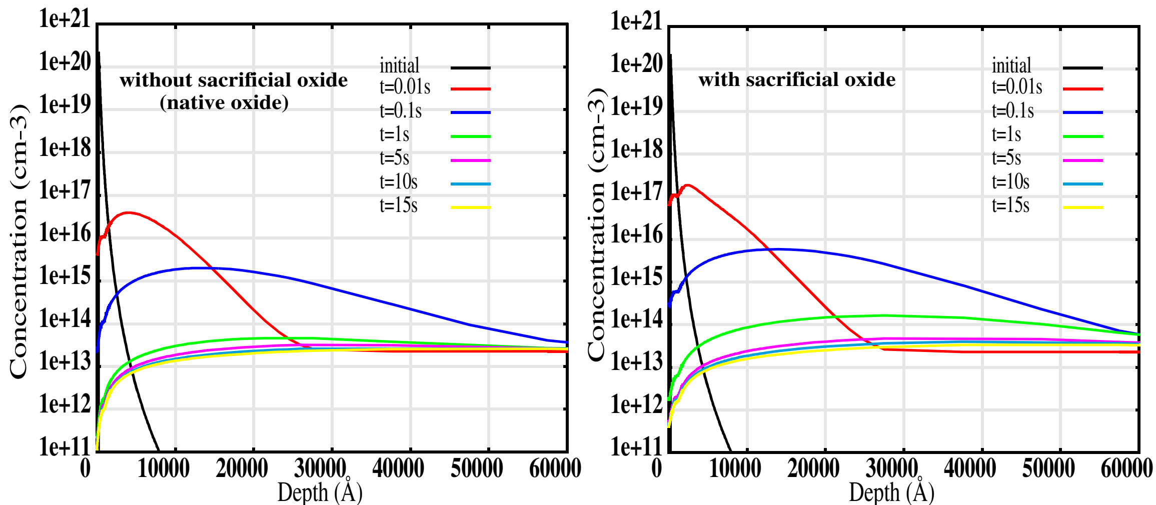

Figure 4. Evolution of the simulated profile of interstitials during the annealing (comparison with or without SACOX)

Since POED could correctly be modelled using the simulator, the next step is to investigate this effect on full 2D process and device simulations.

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IV. ANTICIPATION ON DEVICE PERFORMANCES WITH 2D SIMULATIONS

From process simulations of CMOS, calibrated on the standard 90nm process flow at STMicroelectronics. The drawn gate length was 0.12µm. The activation annealing was a classical RTA, the activation of the surface recombination model with either k1 or k2 to emulate the presence or not of a sacrificial oxide has been introduced.

The doping profiles along the channel, with and without sacrificial oxide, are shown on figure 5**.** Using no oxide results in a longer effective metallurgic gate length (with POED: 50nm, without POED: 66nm).

In terms of electrical performances (figure 6), the transistor is better controlled when no sacrificial oxide is grown in the S/D area: a gain of 95mV is observed on the threshold voltage , the Drain Induced Barrier Lowering (DIBL) was found about 90mV with thermal oxide and 42mV with native oxide.

The leakage is also improved: the OFF state current is decreased by about 30%.

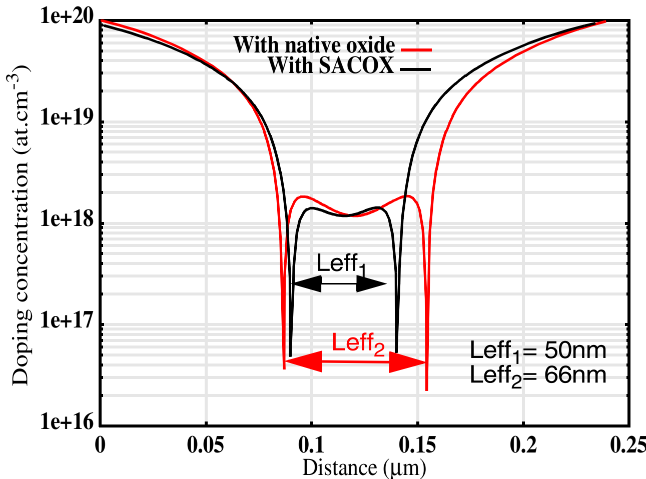
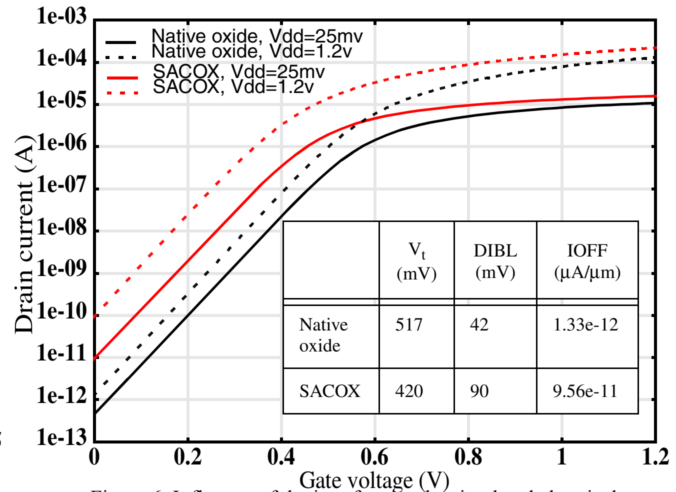


Figure 5. Doping profile along the channel (2nm below the interface SiO_2/Si)



	V_t (mV)	DIBL (mV)	IOFF (µA/µm)
Native oxide	517	42	1.33e-12
SACOX	420	90	9.56e-11

Figure 6. Influence of the interface on the simulated electrical characteristics of the PMOS

V. CONCLUSION

In this paper, the Post Oxidation Enhanced Diffusion evidenced by [2] is modelled by TCAD. The strategy was to use a simple interface recombination model avalaible and to calibrate only the recombination rate depending on the presence or not of an oxide, all the other parameters were kept constant. Experimental profiles could thus be reproduced accurately by 1D simulations. Then, this model was introduced in 2D simulations of a PMOS using a standard 90nm CMOS process flow in order to evaluate the consequences of the POED on the performances of the device. By simulation, the gain found in terms of DIBL was huge (about 50% in reduction).

In this study, TCAD was involved in the development of the technology to evaluate the interest of a new solution (anticipation, cost reduction) and to motivate the experiment on a dedicated lot. Thus, by removing the oxide from the surface before the activation annealing, the diffusion can be reduced by 20nm (with a standard RTA). This low cost solution may be a simple way to optimize the junction depth in the future CMOS technologies.

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