# Simulation of Number of Pulses to Breakdown during TLP for ESD Testing

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***Abstract* — The breakdown characteristics of the gate insulator of nMOSFETs during transmission line pulsing for electrostatic discharge testing is evaluated by using device simulations. Experimental data for the gate bias and gate oxide thickness dependences of the number of pulses to breakdown are reproduced by adopting the anode-hole-injection model. The polarity of the gate bias dependence of the breakdown characteristics can be explained by the depletion of the gate electrode.**

***Keywords-ESD; TLP; gate; breakdown; simulation; TDDB; reliability; AHI***

## I. INTRODUCTION

Immunity to the electrostatic discharge (ESD) is one of the important issues to guarantee reliability of LSI. ESD protection devices and circuits are designed considering thermal immunity [1] according to specification of internal circuits against ESD. In particular, guidelines regarding the reliability of the gate insulators of internal circuits become indispensable, as the thickness is scaled down. For ESD testing, transmission line pulsing (TLP) has been used [2][3]. In this study, the number of pulses to breakdown during TLP for ESD testing is simulated to interpret experimental results.

## II. SIMULATION METHOD

Figure 1 shows a schematic of each component of the direct and FN tunneling currents through the gate insulator. The current densities of electrons in the conduction band ($J_{GCC}$) and valence band ($J_{GVC}$) and of holes in the valence band ($J_{GVV}$) are calculated using the WKB approximation and the tunneling currents are fed back to the generation-recombination term of the current continuity equation in our three-dimensional device simulator. The anode-hole-injection (AHI) model is adopted to estimate the time-to-breakdown $\tau_{BD}$. In this model, $\tau_{BD}$=Min($Q_P(t_{OX})/J_{GRH}(r)$), where $Q_P(t_{OX})$ is the hole density for breakdown of the gate insulator as a function of the gate insulator thickness $t_{OX}$[4][5], $J_{GRH}(r)$ is the hole current density distribution generated by the impact ionization caused by tunneling electrons [4], and Min() is the function for determining the minimum value. The simulation results reproduce typical time dependent dielectric breakdown (TDDB) measurements as shown in Fig. 2. We applied the same scheme to interpret experimental TLP results for ESD testing. The number of pulses to breakdown $N_{BD}$ is calculated by dividing $\tau_{BD}$ by the pulse length (100ns in this study).

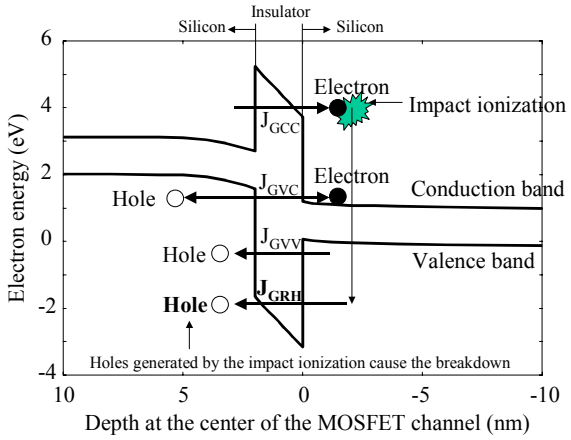


Fig. 1. Schematic of the direct tunneling current through the gate insulator.

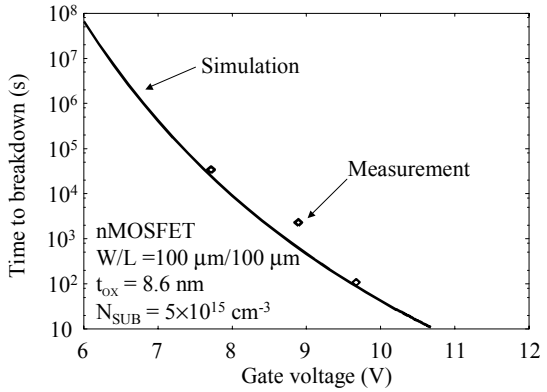


Fig. 2. Comparison of TDDB simulations with measurements.

## III. SIMULATION RESULTS

Figure 3 shows distribution of electron current density at the substrate surface. The density concentrates at edges of the gate and the STI. The AHI around the edges is complicated. $\tau_{BD}$ is estimated by choosing the weakest point as defined by the above expression. Figure 4 shows a schematic of the concentration of electron tunneling. Emission of electrons is enhanced at the shallow trench isolation (STI) edge if the edge

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is sharp, whereas tunneling of electrons is concentrated at the gate edge under the condition of $V_G>0$. Depletion of the gate-poly-silicon depends on the shape of the gate edge. Figure 5 shows the potential distribution around a sharp gate edge in which depletion is ignored. The electric field under the edge is enhanced by the pointed shape of the edge. In contrast, the electric field is relaxed when the gate region is treated as silicon in the device simulation to incorporate the depletion adequately as shown in Fig. 6. The gate depletion is enhanced at the edge, whereas the electric field in the insulator around the edge is relaxed. However, the electron flux from the substrate concentrates at the edge. Therefore the impact ionization is concentrated in the depletion region around the edge. The concentration at the edge is reduced when the edge is extremely rounded by oxidation after forming of the gate by RIE as shown in Fig. 7. A similar electron tunneling concentration is found at the STI edge when $V_G<0$. It is important to carry out simulations considering the edges to include non-uniformities of breakdown probability.

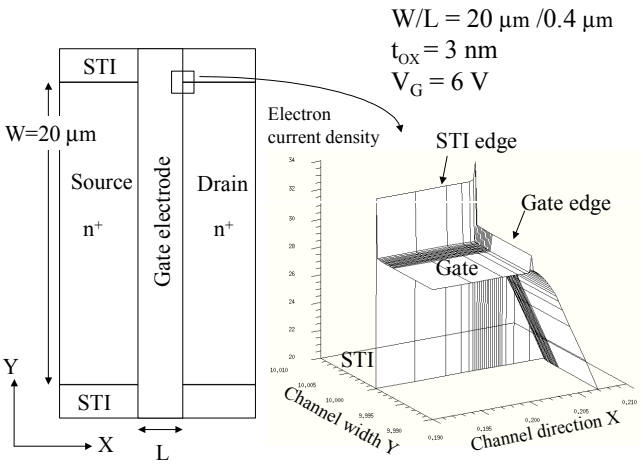


Fig. 3. Distribution of electron current density caused by TLP stress.

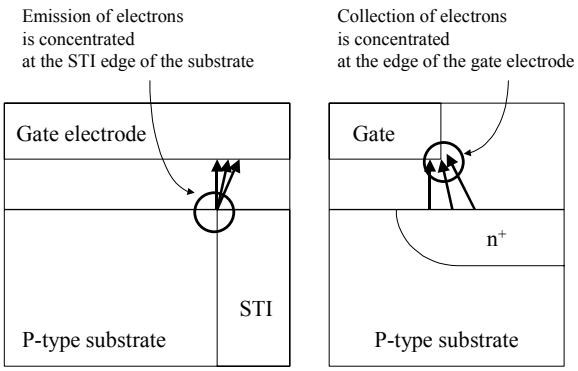


Fig. 4. Schematic of tunneling around the STI and gate edges.

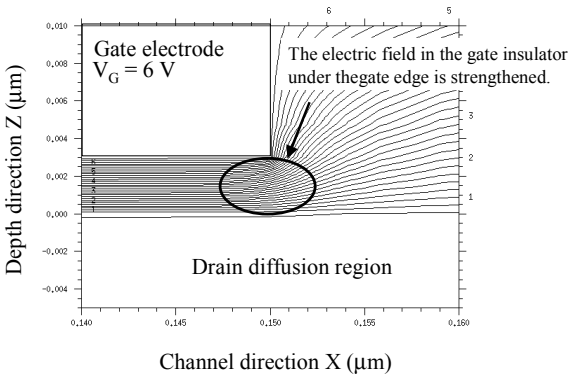


Fig. 5 Potential distribution around a sharp gate edge in which depletion is ignored.

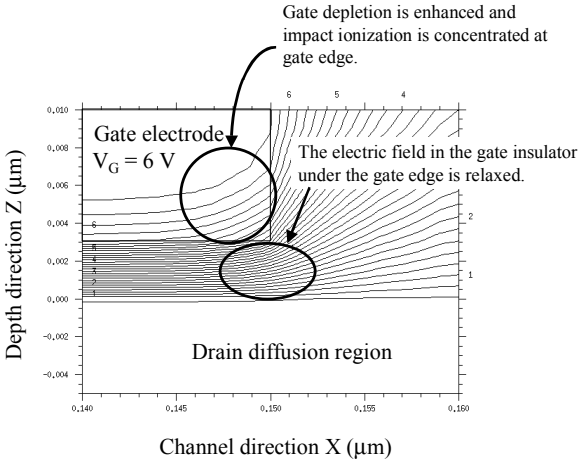


Fig. 6. Potential distribution around a sharp gate edge in which depletion is incorporated.

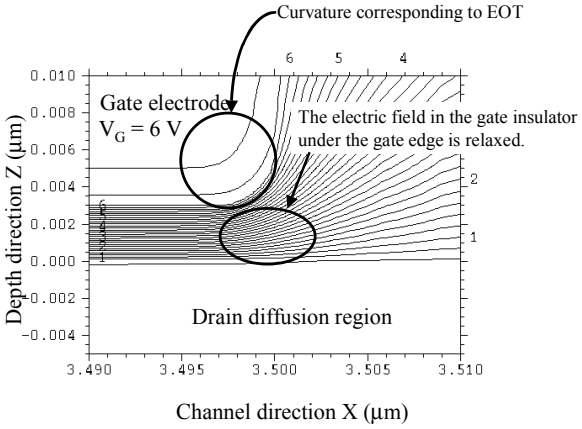


Fig. 7. Potential distribution around a sharp gate edge with curvature corresponding to $t_{OX}$.


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Figure 8 shows the gate bias dependence of each energy component of the gate current. It is found that each component for $t_{OX}$=6 nm at $V_G$>0 becomes lower than that at $V_G$<0 as the absolute value of $V_G$ increases. This can be explained based on gate depletion as outlined below. This dependence of the gate current on the polarity of the gate bias affects the number of pulses to breakdown $N_{BD}$. The component of the valence band electrons becomes significant as $t_{OX}$ decreases and the gate bias increases. Therefore, the influence of the component on the reliability becomes significant.

Figure 9 shows the gate bias dependence of $N_{BD}$. The simulation results reproduce the trends observed in the tendency of measurements. For samples with $t_{OX}$=6 nm, $N_{BD}$ at $V_G$>0 becomes larger than that at $V_G$<0 as the gate bias increases. Namely, the reliability at $V_G$>0 becomes higher than that at $V_G$<0. This is because gate depletion does not take place at $V_G$<0 in nMOSFETs. Figure 10 shows the energy band diagram for the conditions of $V_G$=±10 V. The potential drop in the gate insulator at $V_G$=10 V is larger than that at $V_G$=−10 V, because the effect of the offset due to the built-in potential remains. Figure 11 shows that $V_{OX}$ at $V_G$=14 V is smaller than that at $V_G$=−14 V, because the potential drop in the gate depletion layer becomes significant at $V_G$=14 V and the influence of the built-in potential is canceled. For samples with $t_{OX}$=3 nm, the polarity of the gate bias is not significant. The $V_{OX}$ decreases as the thickness of the gate insulator is scaled down and becomes insensitive to the gate bias polarity as shown in Fig. 12.

Figure 13 shows the relationship between the total electric field $E_{TOT}$ and the intrinsic electric field $E_{INT}$ for three different $t_{OX}$ values. Here $E_{TOT}$ is calculated by dividing $V_G$ by $t_{OX}$ and $E_{INT}$ is calculated using the potential drop in the gate insulator $V_{OX}$ obtained by device simulation. It can be seen that $E_{INT}$ decreases as $t_{OX}$ decreases when $E_{TOT}$ is constant and that $E_{INT}$ is lower at $V_G$>0 than at $V_G$<0. Thus the intrinsically applied electric field must be taken into consideration when evaluating the reliability of the gate insulator.

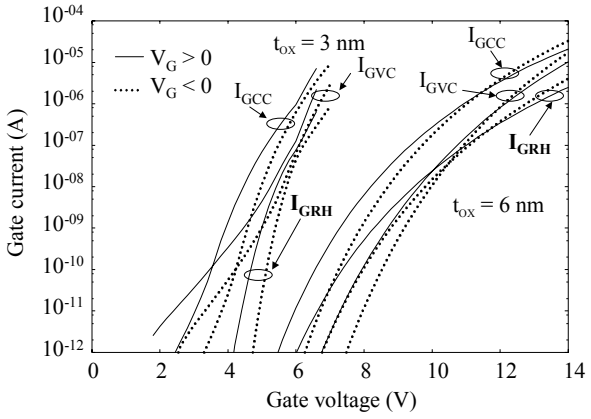


Fig. 8. Gate bias dependence of each energy component of the gate current.

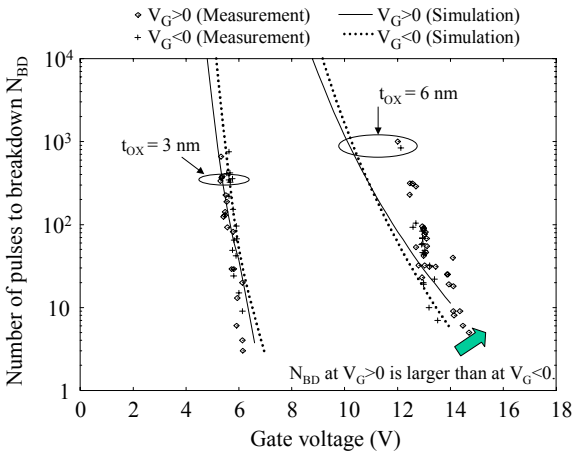


Fig. 9. Gate bias dependence of the number of pulses to breakdown.

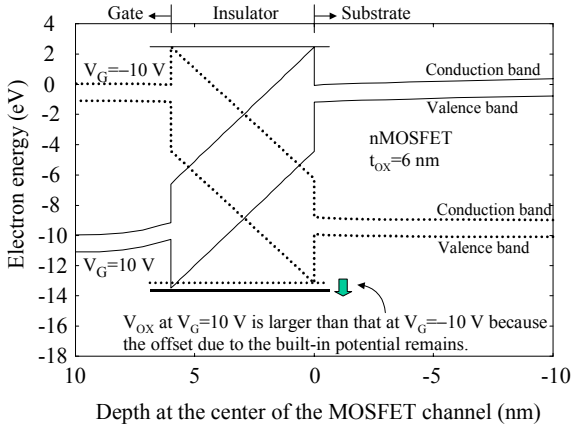


Fig. 10. Energy band diagram at the center of the channel for an nMOSFET with a thick gate insulator at $V_G$=±10V.

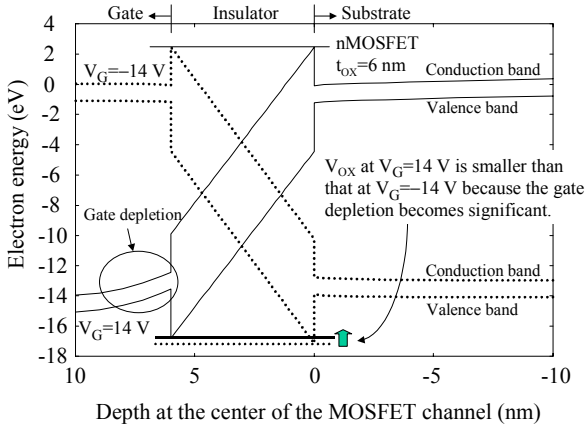


Fig. 11. Energy band diagram at the center of the channel for an nMOSFET with a thick gate insulator at $V_G$=±14V.


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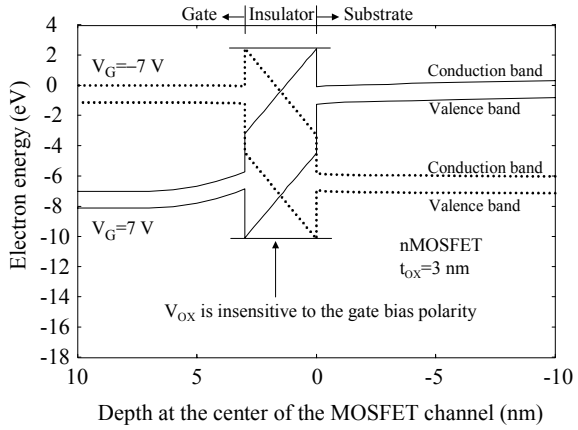


Fig. 12. Energy band diagram at the center of the channel for an nMOSFET with a thin gate insulator at $V_G=\pm 7V$.

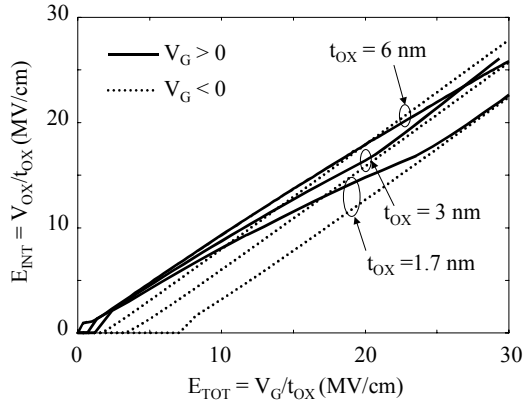


Fig. 13. Relationship between the total electric field $E_{TOT}$ and the intrinsic electric field $E_{INT}$.

## IV. SUMMARY

The number of pulses to breakdown during ESD testing was simulated based on the anode-hole-injection model that was implemented in a device simulator. The gate bias dependence trends of the number of pulses to breakdown were reproduced successfully. It was found that gate depletion affects the polarity of the gate bias dependence of the breakdown characteristics.

## ACKNOWLEDGMENT

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