Coupled Atomistic 3D Process/Device Simulation Considering Both Line-Edge Roughness and Random-Discrete-Dopant Effects

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***Abstract*— We developed new simulation tools for the precise design of sub-100nm MOSFETs. The intrinsic statistical nature of these devices is expressed as fluctuations in device characteristics. Line-edge-roughness (LER) is incorporated in the structural variations in polysilicon gate masks for halo and source/drain-extensions implantations. The statistical nature of these discrete dopant distributions can be automatically included in the simulation by using Monte Carlo procedures for ion implantation and dopant diffusion/activation processes with different computationally generated LER patterns for each individual device. Our 3D device simulations were based on the classical drift-diffusion approach in which electrostatic potentials are constructed from the long-range Coulombic components of individual dopant atom potentials. Using a 3D atomistic approach to both process and device simulation enabled us to closely examine the coupling effects of the most significant sources of fluctuation, i.e. *line-edge-roughness* and *random-discrete-dopants* in the context of practical fabrication processes.**

I. Introduction

Intrinsic random variations in sub-100nm MOSFET device characteristics in addition to any global fabrication process fluctuation are considered to place significant limits on further aggressive device scaling. Gate poly-silicon line-edge-roughness (LER) is one of significant fluctuation sources and LER specifications are thus becoming critical in choosing suitable process technologies, especially for lithography and etching.

Several studies have already reported these problematic LER effects using experimental or simulation approaches[1]-[4]. Due to the lack of reliable 3D tools, however, most previous LER simulations have been restricted to performing 2D slice simulations, although the 3D effects are inherently not small. In addition, the previous studies have treated LER as merely a gate-length modulation, although dopant distributions are undeniably also affected by LER and randomness coupled with the LER should have been simultaneously evaluated on the same simulation platform.

We have developed a new atomistic process simulation program featuring a LER model, which enables us to closely examine the coupling effects of LER and random-discrete-dopant fluctuations.

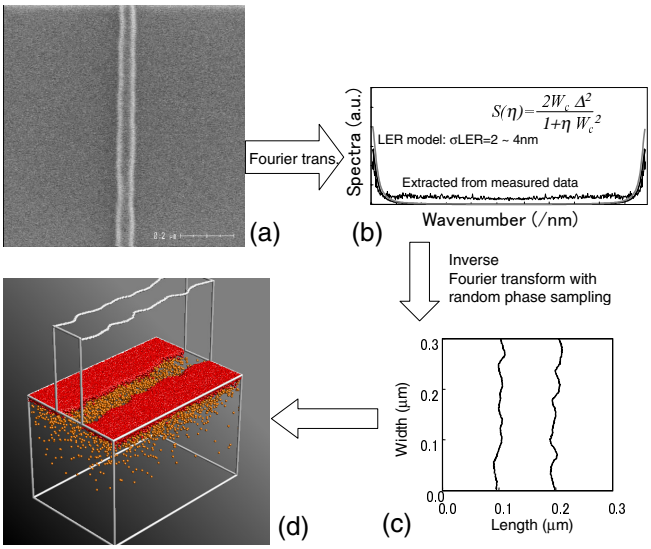

Fig. 1. Simulation procedure incorporating LER. (a) Extract line-edge shape. (b) Fit autocorrelation function power spectrum to the data in Fourier transform. (c) Re-generate line-edge patterns by inverse Fourier transform. (d) Use each line-edge pattern as a mask polysilicon gate shape for ion implantation simulation.

II. Modeling

In this work, LER was incorporated in the polysilicon gate structures, *i.e.* in structural variations in both the gate-electrode and mask for halo- and source/drain-extension implantation. Different random gate-edge patterns were generated based on a method that used autocorrelation functions[4]. The power spectrum was extracted from the actual polysilicon line structural data.

Figure 1 shows a typical simulation procedure incorporating LER. The process is as follows: (a) extract the line-edge shape from actual SEM photograph data, (b) fit the power spectrum of the autocorrelation function to the real data (in Fourier transformed), (c) re-generate the line-edge patterns by inversing the Fourier transform, then (d) use each line-edge pattern as a mask polysilicon gate shape for halo and source/drain implantation.

The typical LER amplitude was found to be 2nm of its

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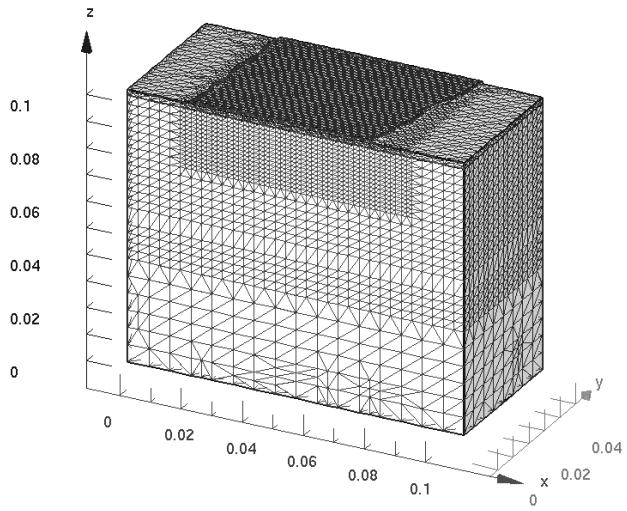

Fig. 2. A typical mesh structure for 3D device simulation. Here, total number of grid point was 35344, and the minimum mesh size was 2nm.

standard deviation. The discrete dopant distributions in MOSFETs were calculated using an atomistic process simulation program[6]. The implantation and diffusion models incorporated in this process simulation code were validated by comparing them with various boron spike-anneal experiments[7].

The statistical nature of the discrete dopant distributions can be automatically included in this simulation by using Monte Carlo procedures for ion implantation and dopant diffusion/activation processes with different, computationally generated LER patterns for each individual device. When the ion implantation process is simulated, our Monte Carlo program handles a sampling weight of each ion to reproduce an actual implantation dosage. Incident ion penetration through a gate polysilicon edge and a gate-oxide, for oblique angled halo implantation, was also considered.

The 3D device simulations were performed based on the classical drift-diffusion approach in which electrostatic potentials are constructed from the long-range Coulombic components of the individual dopant atom potentials[5]. A screening length, i.e. a criterion for separating long-range Coulombic components, was derived from an ensemble Monte Carlo/Molecular Dynamics carrier mobility calculation so as to avoid a double counting problem of screening effects[5]. The device simulation main program used in this work was HyDeLEOS developed by SELETE[8]. We have made two major modifications on the original HyDeLEOS. One was the abovementioned atomistic electrostatic potential incorporation including an interface between our atomistic process simulation program. The other was an incorporation of efficient 3D non-uniform grid generation method[9]. Our 3D tetrahedral mesh that satisfies the Delaunay criterion provides efficient local discretization ways to reduce total computation time. Figure 2 shows a typical mesh structure used in this simulation. Only the selected region including a MOSFET channel was divided into fine meshes which have typically an interval of 2-nm.

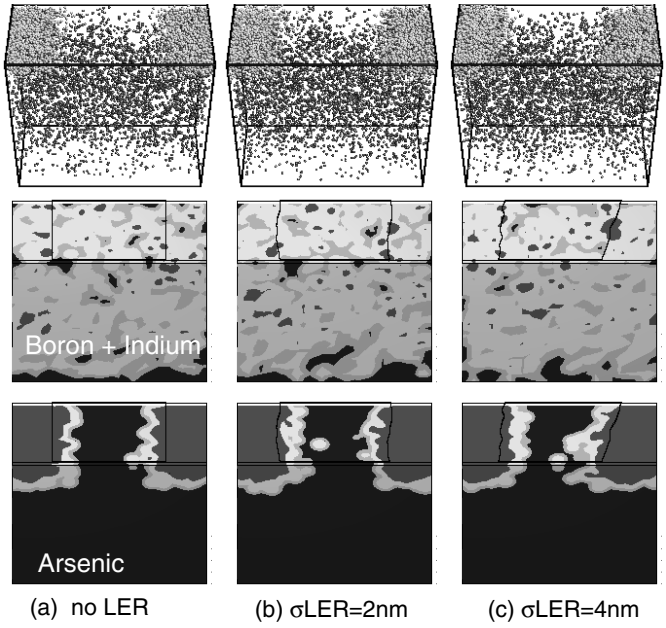

Fig. 3. Monte Carlo implantation/diffusion simulation results with different LER amplitudes. Boron was used for channel doping, indium was used for halo 30-degree tilted implantation, and arsenic was used for source/drain-extensions. It should be noted that the random-discrete-dopant effects were automatically included in all these calculations in this work. A fabrication process condition was supposed to be the same for all the sampling devices.

III. Results and Discussions

This simulation system was applied to sub-100nm super-halo designed MOSFETs. The super-halo structure is supposed to be fabricated using tilted implantation counter-doping prior-to source/drain-extension implantations.

Typical gate length (Lg) values were 65nm and 45nm. Device characteristics were simulated for various LER specifications, typically changing the standard deviation of LER from 0nm (no LER) to 4nm, as shown in Figure 3. Boron was used for channel doping, indium was used for halo 30-degree tilted implantation, and arsenic was used for source/drain-extension doping. All the implantation processes were simulated using a Monte Carlo ion implantation simulation program, and subsequent diffusion and activation during spike annealing were also calculated using a kinetic Monte Carlo diffusion simulation program. It should be noted that random-discrete-dopant effects were automatically included in all these calculations in this work. The recipe for the fabrication process conditions, such as ion implantation energy, dose, and annealing temperature/time was the same for all the sampling devices.

Figure 4 shows the calculated on-(off-)current (I_{on}, I_{off}) distributions of 80 identical but statistically different devices in terms of LER and random-discrete-dopants. Overall, the fluctuation originating from the random-dopant-distribution was found to be the dominant factor in device fluctuations. The simulation results also showed that LER increases I_{off} for devices with shorter gate length. As shown in Figure 4, LER gives rise to broadening of the distribution plots toward

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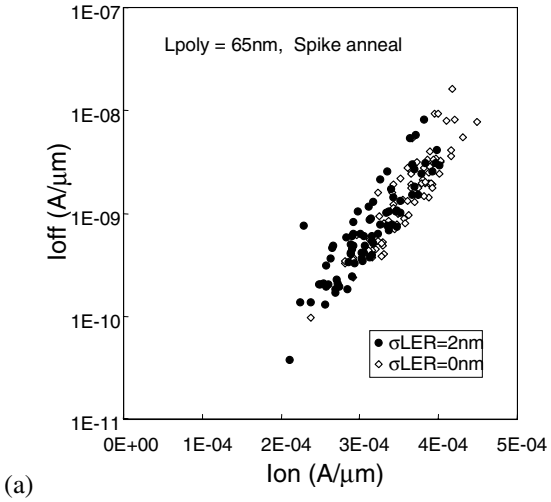
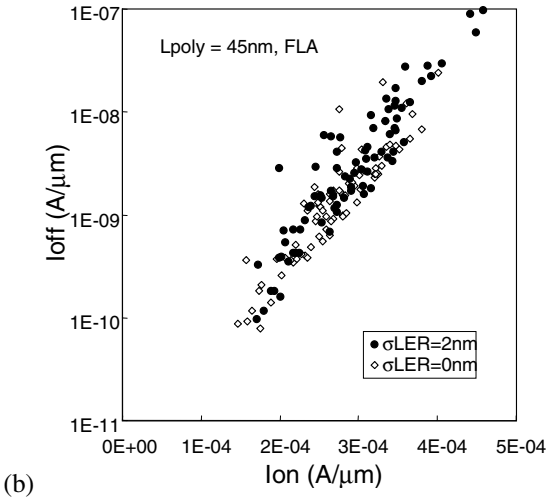


(a)



(b)

Fig. 4. Simulation results for on-current and off-current distributions obtained from devices of (a) Lg=65nm and (b) Lg=45nm, with and without LER. LER gives rise to broadening of distribution plots toward I_{off} enlarged.

I_{off} enlarged, and this I_{off} enlargement is shown to be larger with a gate length of 45nm than with a gate length of 65nm. This strongly suggests that a reduction in LER can produce a gain in drive-current for devices with a gate length of less than 45nm.

The simulation results show that LER gives an average threshold voltage (V_{th}) shift according to the V_{th}-L characteristics of the corresponding device design as shown in Figure 5. It was also found that LER not only modulates Lg but also increases halo-implantation effective dose amounts because it effectively increases the mask side-wall area for a large-angle tilted halo-implantation. Consequently, Lg=65nm devices showed a positive shift of average V_{th} as shown in Figure 6(a), while a negative average V_{th} shift is seen for Lg=45nm devices, as shown in Figure 6(b).

The simulation results also indicate that LER enhances V_{th} fluctuation in addition to the random-discrete-dopant effects. Figure 7 shows the calculated average threshold voltages and their standard deviations for devices calculated with or

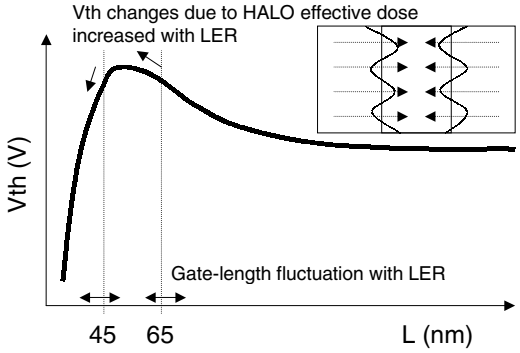


Fig. 5. Diagram showing how LER affects threshold voltage changes. LER not only modulates channel length but also increases large-angle halo-implantation dosage because of effective enlargement of mask side-wall area.

without LER. The simulation analyses also revealed that some diffusion-less annealing processes such as the extremely short time annealing technique called flash-lamp-annealing (FLA) can enhance the fluctuation arising from LER, as shown in Figure 7(b). As Figure 8 shows, this is because the dopant distributions underneath the gate edges correlate well to the edge-fluctuating shapes that occur with diffusion-less annealing cases, while dopant diffusion during conventional spike-annealing smoothes the source/drain-extension edge, which moderates the susceptibility of device performance to LER. This finding provides additional motivation for reducing LER in future sub-50nm devices.

IV. Conclusion

The coupled 3D atomistic process/device simulations described have been shown to be suitable for application to sub-100nm MOSFETs in which intrinsic fluctuations play a significant role in limiting improvements in device performance. In particular, using atomistic process simulation to examine LER enables us to obtain non-trivial insights that will be useful in further optimizing the design of fabrication processes.

Acknowledgment

The authors would like to thank Dr. A. Ono, NEC Electronics Corporation, for providing SEM photograph and for valuable discussions.

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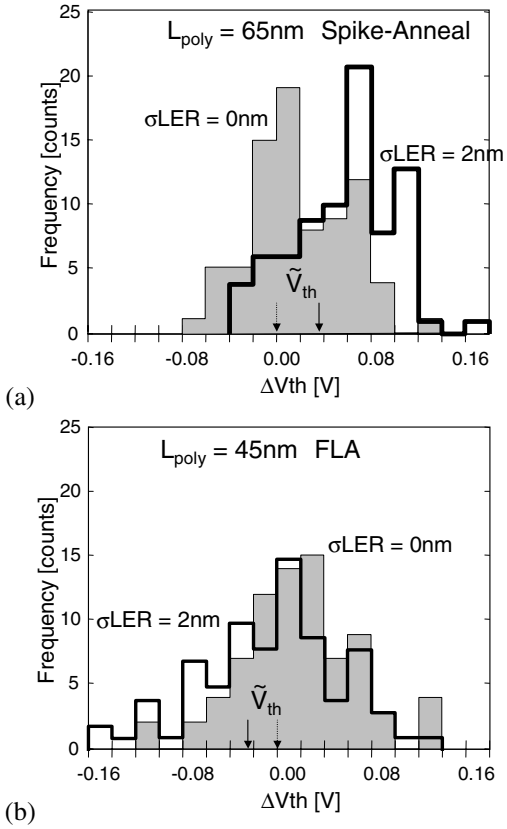

Fig. 6. Simulation results for individual device threshold voltage distributions. LER gives rise to average Vth shifts according to the corresponding device V_{th}-Lg characteristics.

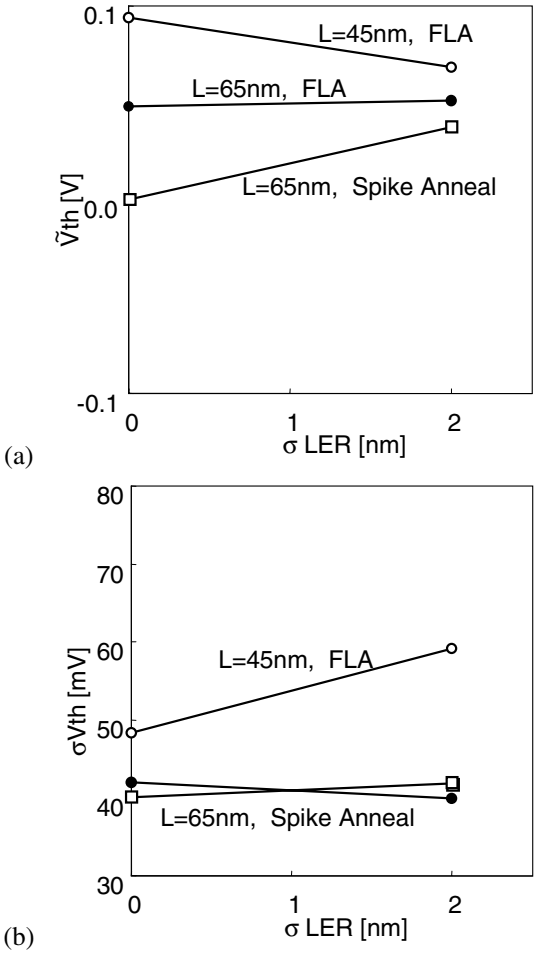

Fig. 7. (a) Calculated average threshold voltages, and (b) standard deviation values for devices with and without LER. Annealing process conditions assumed here are 1050℃ spike-annealing and 1200℃ flash-lamp-annealing(FLA)[7], respectively.

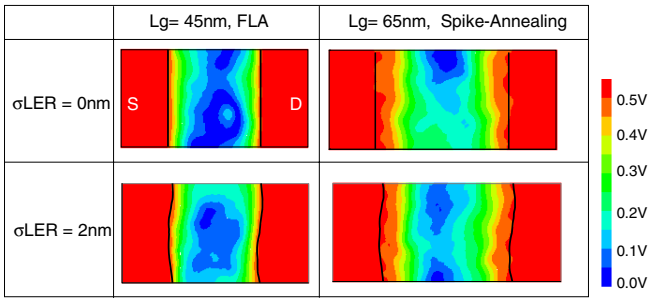

Fig. 8. Calculated electrostatic-potential distribution on device surfaces. For the diffusion-less annealing cases (Lg=45nm, FLA), source/drain potential edge shape is seen to be aligned well to the gate-edge fluctuated shapes while dopant diffusion (Lg=65nm, spike-annealing) disturbs this correlation.