Hydrodynamic Simulation of RF Noise in Deep-Submicron MOSFETs

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***Abstract*—A noise model for MOSFETs based on analytical microscopic noise sources has been developed and noise simulations based on the hydrodynamic model have been performed. The drain and gate excess noise parameters and correlation coefficient are extracted and the reasons for noise parameter dependence on the channel length are explained.**

Keywords-hydodynamic;drain noise;gate noise;correlation coefficient; impedance field; local noise source

I. INTRODUCTION

Due to the continuous scaling of MOSFETs, analog CMOS circuits can now operate in the GHz range and modeling of RF noise in MOSFETs has become an important TCAD topic (e.g.[1]). However, the behavior of this RF noise in deep-submicron MOS devices is not well analyzed and modeled. Recently, a hydrodynamic (HD) noise model has been developed for bulk-transport-dominated devices (i.e. bipolar devices). In this work an HD noise model for Si MOSFETs is presented, which includes a model for surface transport. The HD model is the one of [3] and in contrast to [2] this model is based on an analytical formulation of the microscopic noise sources, which is readily extended to the case of surface transport.

II. NOISE SIMULATION THEORY AND MODEL

The noise at each electrode is calculated similar to the impedance field method. A transfer function between a point $\vec{r}$ in the device and the k-th electrode is defined as:

$$A_k = \frac{i_k}{i_{in}} \tag{1}$$

where i_{in} is the injected current and i_k is the current at the k-th electrode generated by the injected current i_{in}.

The local noise generation can be modeled as injecting a current at a location $\vec{r}$ and pulling out that current from another location $\vec{r}'$ near $\vec{r}$. The contribution to noise at the k-th electrode from location $\vec{r}$ becomes:

$$\left|\nabla A_k\right|^2 S_{in} \tag{2}$$

where S_{in} is the power spectral density of the local noise source (Fig. 1).

Finally, integrating (3) over the whole area of the device gives the total noise at the k-th electrode. Electrons and holes have their own transfer functions, and the integration must be done for each carrier type:

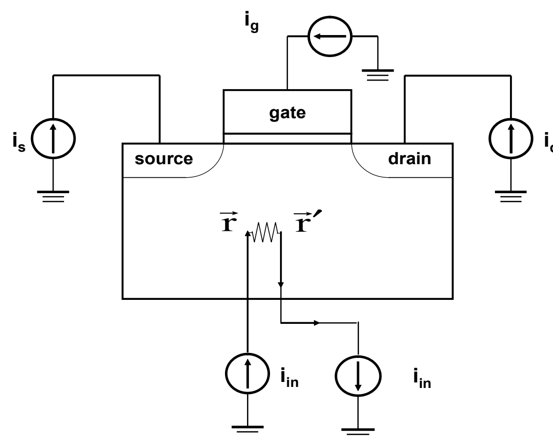

Fig. 1. Basic concept of impedance field noise simulation

$$S_{ik} = \int \left|\nabla A_{nk}\right|^2 S_{in} dv + \int \left|\nabla A_{pk}\right|^2 S_{ip} dv \tag{3}$$

The first term in the above equation represents the contribution to noise from electrons, and the second term the contribution from holes. (In the case of the HD model a more general definition of the transfer function must be used [2].)

In a region where the electric field is very high, the Einstein relation is not correct because we cannot assume quasi-equilibrium anymore. Based on Monte-Carlo simulations the Einstein relation is corrected as:

$$D = \frac{kT_c}{q}\mu(0.4 + 0.6\frac{\mu}{\mu_0}) \tag{4}$$

where μ is carrier-temperature-dependent mobility and μ_0 is the low-field mobility. T_c denotes the local carrier temperature.

The coupling of energy and velocity fluctuations through the Joule term also creates a correction to the local noise source in case of the HD model [2]. Including this coupling effect, the local noise source with those corrections becomes:

$$S_{in} = 4q^2 n\mu v_{T_n}(0.4 + 0.6\frac{\mu}{\mu_0}) \times \left(2 - \frac{1}{1+\alpha(v_{T_n} - v_{T_0})}\right)^2 \tag{5}$$

$$v_{T_n} = \frac{kT_n}{q}, \quad v_{T_0} = \frac{kT_0}{q}$$

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where T_n and T_0 represent the electron and lattice temperature, respectively.

III. RESULTS

In contrast to the drift-diffusion (DD) model HD MOSFET simulations yield for large drain voltages a carrier velocity overshoot near the drain. This velocity overshoot changes the carrier injection condition at the source because the carrier distribution in the device is also changed. This effect results in a larger transconductance and smaller gate-to-source capacitance than those predicted by the DD model. Figs. 2 and 3 show the cutoff frequency evaluated by the HD and DD models for NMOS and PMOS transistors, respectively. The cutoff frequency of a MOS transistor is approximately given by the transconductance divided by the gate-to-source capacitance. Therefore the HD model predicts a far higher cutoff frequency than the DD model. The MOS device used in this simulation has a 90nm metallurgical channel length and 20 Å gate oxide thickness. The channel doping is $5\times10^{17}/cm^3$ and uniform. The difference in the cutoff frequency is larger for the NMOS transistor case, because the electron energy relaxation time 0.3ps and twice as large as the hole energy relaxation time (0.15ps). Therefore the difference between HD and DD simulations is larger in the NMOS case.

Fig. 4 illustrates the relation between the local noise source and carrier temperature. The new local noise source model predicts a fast increment with carrier temperature until 1000K and saturation beyond. In the calculations for Fig 4., $n=5\times10^{17}/cm^3$ and $\mu_0=800\ cm^2/Vs$ were used.

Using this new local noise source model, HD and DD simulations have been performed for MOS transistors with metallurgical channel lengths ranging 90nm to 10μm. Those MOS transistors have the same profile except for variations in the channel length. The gate bias was set to 1.08V for NMOS transistor and –1.07V for PMOS transistor where they have maximum cutoff frequency.

The drain excess noise parameter (γ) for NMOS and PMOS transistors with various channel lengths is shown in Figs. 5 and 6. For a frequency of 1MHz and a channel length of 10μm both simulation models reproduce the analytical result (γ=0.66) for long channel devices in saturation [4]. For 2.5GHz nonquasistatic effects occur in the long channel devices and the drain noise increases [1]. In the case of the short channel devices these effects occur at much higher frequencies and no differences are found for the two frequencies shown. For channel lengths below 1μm the noise increases for short channels. The maximum drain noise parameter is 1.76 for NMOS and 1.53 for PMOS from HD simulations and in good agreement with recent experimental results [1]. While the result from the HD model increases for shorter channels, that from the DD model slightly decreases, indicating that excess noise is generated by nonequillibrium effects. The drain noise versus gate bias is shown in Fig. 7.

In Figs. 8 and 9 the gate excess noise factor (δ) for various channel lengths is shown. The gate noise parameter increases rapidly in short channel devices. For the 90nm channel length devices, the HD model predicts 5.36 for NMOS and 3.49 for PMOS transistors. The gate noise versus gate bias for the 90nm channel length device is shown in Fig. 10.

Figs. 11 and 12 show results for the imaginary part of the correlation coefficient between gate and drain noise currents (Im(c)). Im(c) decreases with channel length in the HD model while it increases slightly in the DD model. The HD result agrees well with experimental result [6].

The imaginary part of the correlation coefficient (Im(c)) is a strong function of the gate bias. Fig. 13 shows the relation of Im(c) and gate voltage. Im(c) increases with gate bias and has a peak at 0.13V. After that, Im(c) decreases with gate bias. The HD model consistently predicts smaller Im(c) and at 1.2V gate voltage, Im(c) drops to 0.208 which is approximately half of the long channel value (0.395) [5].

The local contribution to drain noise from the channel is shown in Fig. 14. The HD model predicts higher drain current noise and higher contributions from the channel. The peak contribution is located near the source, not drain, and that means that the high energy electrons created by the large electric fields near the drain are not the direct origin of excess noise. The gradient of the transfer function for drain noise near the drain junction is very small and the local noise near the drain cannot contribute to the total drain noise. Moreover, the source side has a higher carrier concentration and larger local noise source. Consequently, the excess drain noise is created by the change in the transfer field and the larger local noise source due to the higher carrier concentration.

Fig. 15 shows the local contribution to gate noise from the channel. We can notice that there are two peaks in Fig. 15, one is near the source, and one is near the drain. The gradient of the transfer function for gate noise has an 'M' shape and, unlike drain noise, the excess gate noise is mainly from the high energy electrons near the drain.

The difference of excess noise mechanism for drain current noise and gate current noise creates the reduction of the correlation coefficient. Fig. 16 shows the contribution to the imaginary part of the correlation coefficient from the channel. The source side contribution is positive and the drain side one negative. As the channel length reduces, the drain side starts to create more gate noise and enhances the negative contribution. Finally, those two opposite contribution to Im(c) cancel out and Im(c) decreases.

IV. CONCULSION

A general HD noise model for MOSFETs based on analytical microscopic noise sources has been developed. In the long channel case for saturation the results of the analytical models are recovered under quasistatic conditions. In the short channel case experimental trends are reproduced and for 90 nm MOSFETs, a drain excess noise factor of 1.76 (N), and 1.53(P) and a gate excess noise factor of 5.36(N) and 3.49(P) was found.

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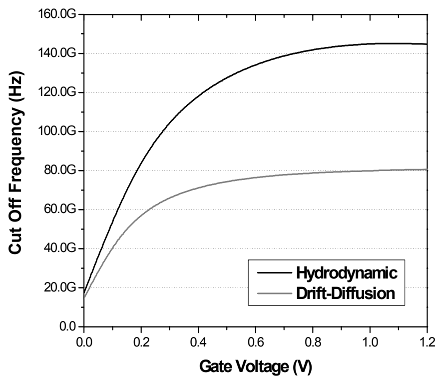

Fig. 2. Cut-off frequency calculation result for 90nm channel length NMOS transistor. Vd=1.2V

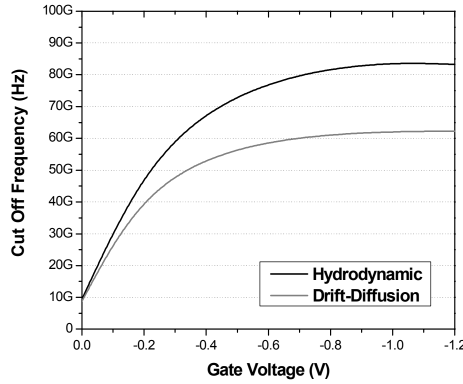

Fig. 3. Cut-off frequency calculation result for 90nm channel length PMOS transistor. Vd=-1.2V

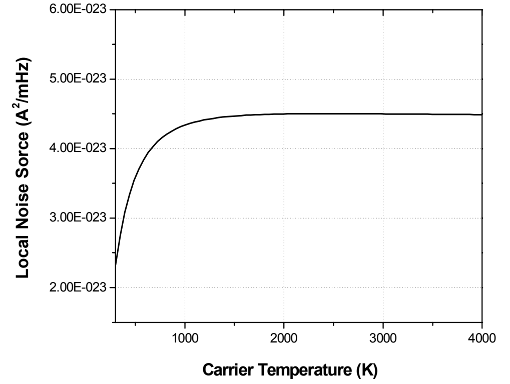

Fig. 4. Relation of local noise source and local carrier temperature. $n=5\times10^{17}/cm^3$ and $\mu_0=800\ cm^2/Vs$

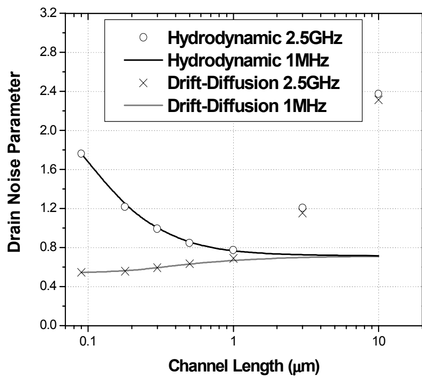

Fig. 5. Drain noise parameter (γ) dependence on channel length reduction for NMOS transistors. Vg=1.08V and Vd=1.2V

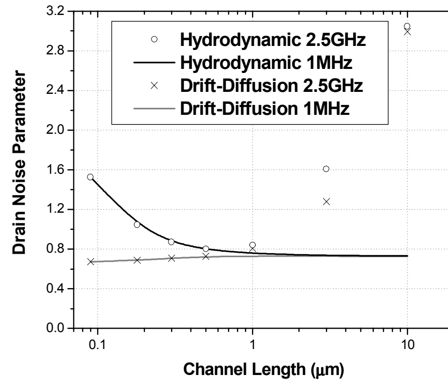

Fig. 6. Drain noise parameter (γ) dependence on channel length reduction for PMOS transistors. Vg=-1.07V and Vd=-1.2V

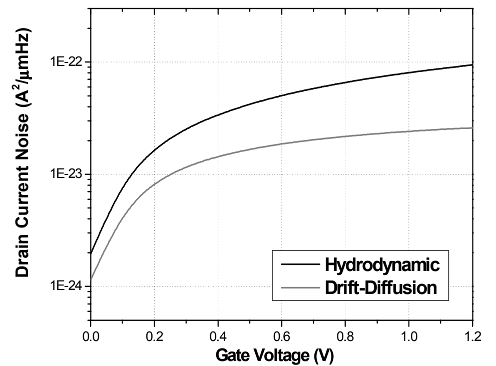

Fig. 7. Drain noise for 90nm channel length NMOS transistor. Vd=1.2V

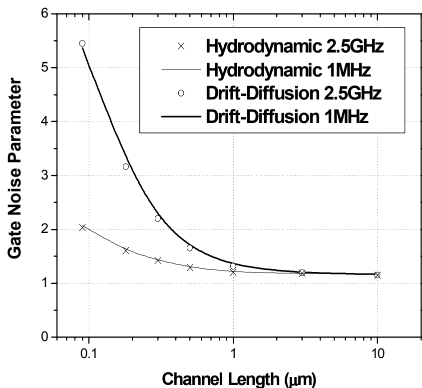

Fig. 8. Gate noise parameter (δ) dependence on channel length reduction for NMOS transistors. Vg=1.08V and Vd=1.2V

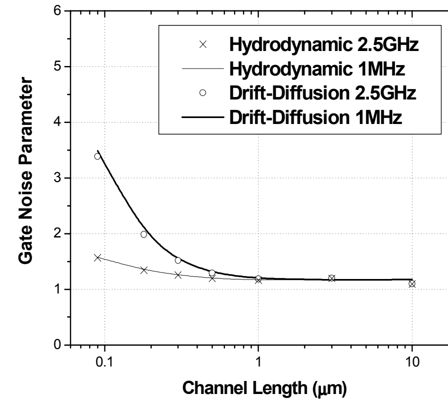

Fig. 9. Gate noise parameter (δ) dependence on channel length reduction for PMOS transistors. Vg=-1.07V and Vd=-1.2V

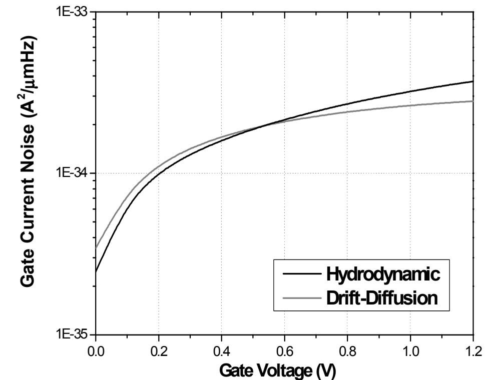

Fig. 10. Gate noise for 90nm channel length NMOS transistor. Vd=1.2V

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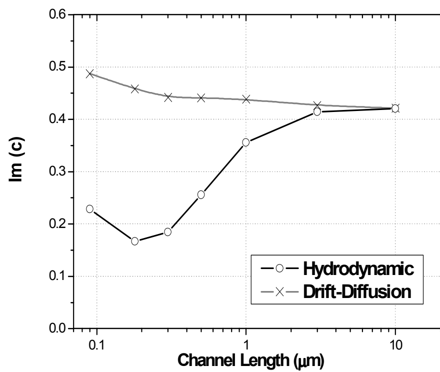

Fig. 11. Relation of imaginary part of correlation coefficient between gate and drain noise (Im(c)) with channel length for NMOS transistor. Vg=1.08V and Vd=1.2V

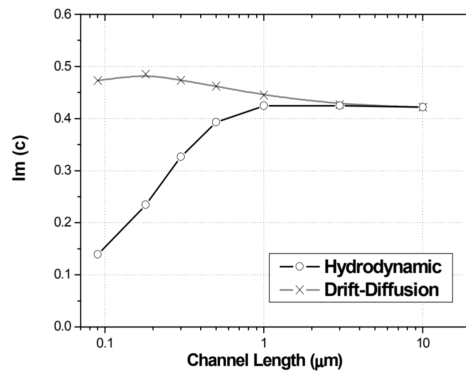

Fig. 12. Relation of imaginary part of correlation coefficient between gate and drain noise (Im(c)) with channel length for PMOS transistor. Vg=-1.07V and Vd=-1.2V

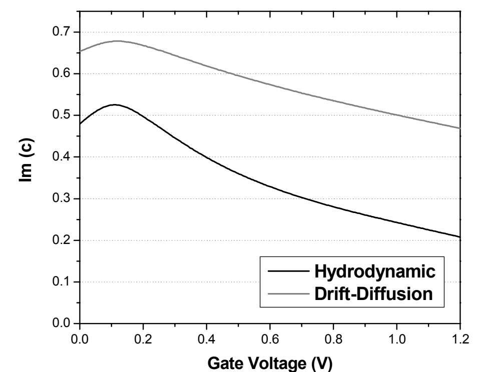

Fig. 13. Reduction of imaginary part of correlation coefficient between gate and drain noise (Im(c)) by gate bias. Vd=1.2V

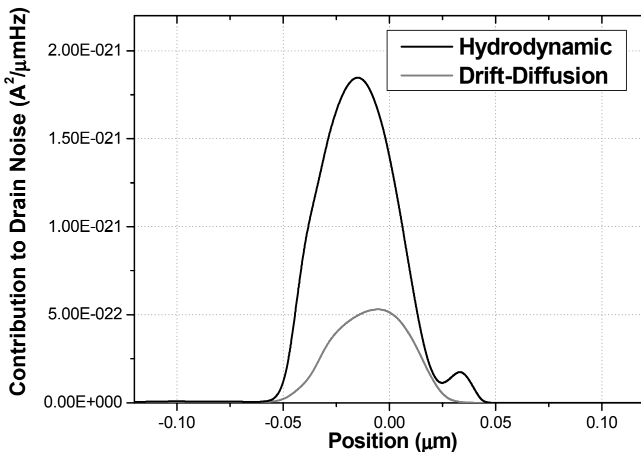

Fig. 14. Local contribution to drain noise at for 90nm channel length NMOS transistor. Vg=1.08V and Vd=1.2V

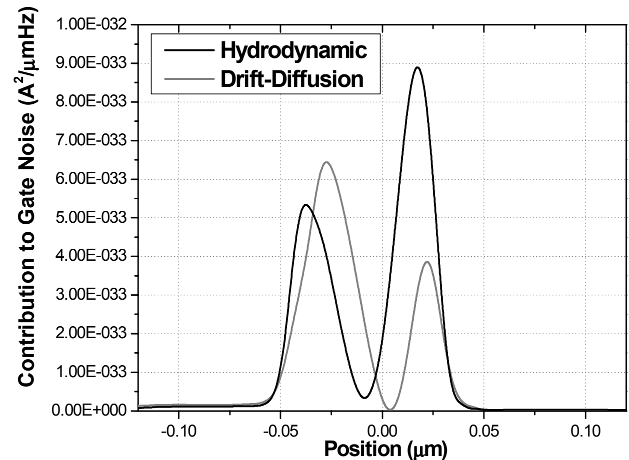

Fig. 15. Local contribution to gate noise for 90nm channel length NMOS transistor. Vg=1.08V and Vd=1.2V

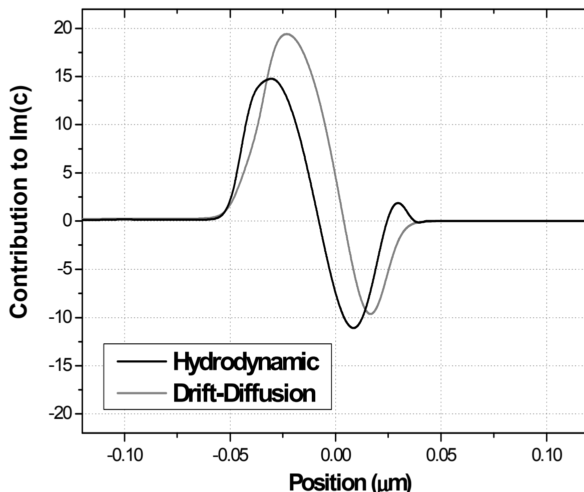

Fig. 16. Local contribution to imaginary part of correlation coefficient between gate and drain noise (Im(c)) for 90nm NMOS transistor. Vg=1.08V and Vd=1.2V

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