Thermal Noise Modeling for Short-Channel MOSFET's

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***Abstract*—In this work, a physics-based MOSFET drain thermal noise current model valid for all channel lengths was presented for the first time. The derived model was verified by extensive experimental noise and charge measurement of devices with channel lengths down to 0.18 μm. Excellent agreement between measured and modeled drain thermal noise was obtained for the entire V_{GS} and V_{DS} bias regions.**

Keywords: thermal noise, MOSFET, velocity saturation effect, inversion charge, channel length modulation

I. INTRODUCTION

Due to large enhancement of drain current thermal noise of short-channel MOSFET reported in the two decades ago compared to long-channel theory [1], there are many literatures to try to explain such the increase by introducing hot electron effect in velocity saturation region. Abidi [2] initially reported that the noise excess factor was up to 8 in the device with 0.7 μm channel length. Therefore, the thermal noise for short-channel MOSFETs has attracted many attentions. However, recently many experimental and simulation works have addressed that the generated noise due to hot electron in the velocity saturation region is negligible [3]. But controversies about the noise behavior in short-channel have not been fully solved yet.

We suspect that the part of this controversy originates from the measurement in accuracy. It is not easy to measure the noise for the short channel intrinsic device very accurately. It is always important to confirm whether the obtained noise data was measured accurately or not. Many previous results have addressed the thermal noise only at saturation region. However, since the change of thermal noise with drain bias is most prominent in the linear region, noise measurement and modeling in the linear region is very important to obtain basic insight of noise behavior. Especially, noise comparison between theory and experiment at $V_{DS} = 0$ V is very important for checking measurement accuracy as well as noise calibration. As far as we know, drain noise measurement covering entire V_{DS} regions has never been reported for short channel MOSFETs.

In addition, velocity saturation effect should be considered to model the drain thermal noise for short channel MOSFETs. The effect deviates the formulation of thermal noise for short-channel from the approach used in the long channel. In this work, the noise model including velocity saturation effect is presented and verified with extensively measured and carefully checked noise data from linear to saturation regions.

II. THERMAL NOISE MODEL

The channel of a MOSFET is divided into two regions. One is the so called gradual channel region with length of L_{eff} - ΔL and the other is velocity saturated region with length of ΔL. With the assumption that the gradual channel region has constant mobility and that drain noise current can be calculated using the impedance field method, Y. Tsividis [4] derived the analytic model

$$<i_{int}^2>=4kT_o\Delta f\frac{\mu_{eff}}{(L_{eff}-\Delta L)^2}Q_{inv} \quad (1)$$

,where T_o is ambient temperature, Δf is measurement bandwidth, μ_{eff} is the effective mobility, L_{eff} - ΔL is the length of gradual channel region, and Q_{inv} is the total inversion charge in gradual channel region. Note that equation (1) was valid for long channel devices. However, since mobility of carriers in short channel MOSFETs is degraded due to the lateral field, which makes the channel segment nonlinear, we cannot follow Tsividis' approach that is based on thermal noise formulation of linear infinitesimal channel resistor. Therefore, we should formulate the thermal noise based on diffusion noise source [1]. Also the impedance field should be recalculated in case of taking into account velocity saturation effect. With assumption that diffusion coefficient is constant over the channel [5] and the contribution of carriers in velocity saturation region is negligible, we have derived the thermal noise model in short channel MOSFETs and we found that (1) is very accurate model for even short channel device, too. More detailed derivation will be published elsewhere [6]. Note that $L = L_{eff}$ - ΔL is the length of the gradual channel region, not the length of total channel region and μ_{eff} is only gate bias dependent effective mobility, not the mobility including the degradation due to lateral field.

III. NOISE MEASUREMENT AND MODELING

A. The Accuracies of Noise Measurement

The DUT (device-under-test) are n-type MOSFETs with folded gate structure. The unit finger width and the number of finger were 5 μm and 16, respectively. The drain thermal noise of MOSFET with channel lengths of 0.5, 0.35, 0.25, and 0.18 μm, were measured and extracted. Noise parameters and scattering parameters were measured by ATN noise and HP S-parameter measurement setup in frequency range from 3 GHz to 6 GHz. To check the noise measurement accuracy, we first measured extrinsic drain noise current at $V_{DS} = 0$ V, which should be equal to $4kT_o\Delta f \cdot real(Y_{22})$ from thermodynamic

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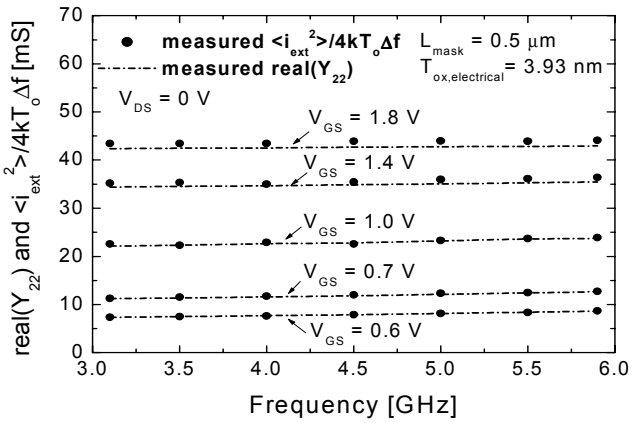

Fig.1. Measured $<i_{ext}^2>/4kT_o\Delta f$ and *real*(Y_{22}) vs. frequency with various V_{GS} at $V_{DS} = 0$ *V*. This figure shows the accuracies of our noise measurement system.

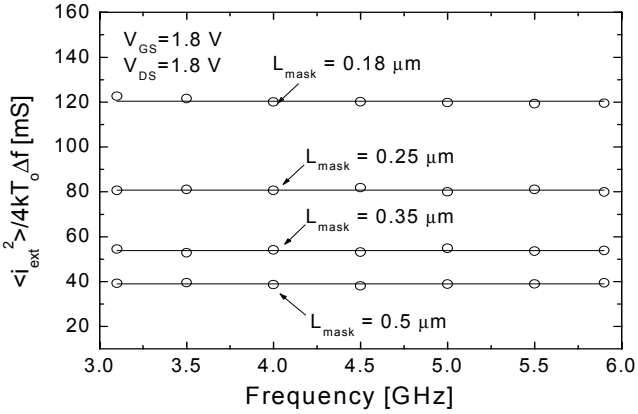

Fig.2. White extrinsic noise sources were measured for the devices with various channel lengths for the frequency from 3 to 6 GHz, which shows the *1/f* noise is negligible. The symbol represents measured data and the line represents the average value.

theory, where Y_{22} is independently measured using S-parameter set-up. Note that *real*(Y_{22}) is determined by the channel conductance of MOSFET and the source/drain resistance dominantly. It was confirmed that $<i_{ext}^2>/4kT_o\Delta f$ is nearly equal to *real*(Y_{22}) over whole frequency and gate bias range as shown in Fig.1, which not only verifies Nyquist theorem but also demonstrates the accuracy of our noise measurements. And we found the measured drain thermal noise is always white for various channel lengths and biases as shown in Fig.2, indicating that *1/f* noise is negligible in the measured frequency range of 3 GHz ~ 6 GHz.

B. Parameter Extraction

To verify the drain thermal noise model given by (1) for short channel MOSFET, effective channel length (L_{eff}), effective mobility (μ_{eff}), total inversion charge (Q_{inv}) should be obtained. Firstly, the accurate determination of the effective channel length (L_{eff}) is very important. The reduction of channel length ($\delta L = L_{mask} - L_{eff}$), where L_{mask} is the drawn gate length, and series source/drain resistance (R_{sd}) were extracted from the measured ac channel resistance (R_{do}) at $V_{DS} = 0$ V vs. L_{mask} plot as shown in Fig.3 [7]. All the lines were crossed at one point. From the intercept point, we obtained δL = 36.5 nm and R_{sd} = 2.495 Ω.

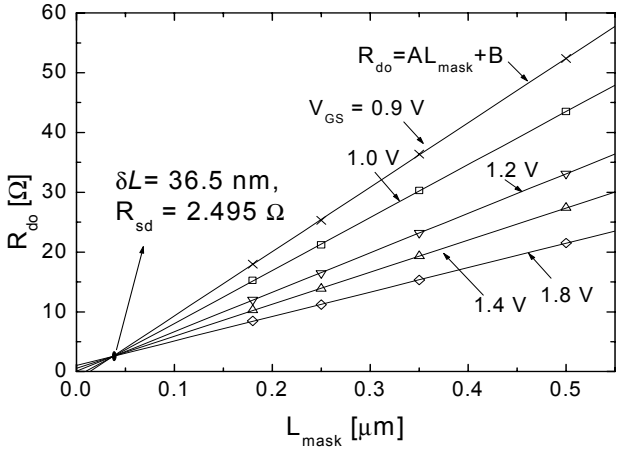

Fig.3. The lines vs. L_{mask} for different gate bias intersected at a single point, which results in bias independent L_{eff} and R_{sd}.

Conventionally, the effective mobility (μ_{eff}) is extracted from long-channel device, where source and drain resistance are negligible. However, in the device with halo implant, the mobility of short-channel device can differ from that of long channel device, because the average substrate doping concentrations are different. We have extracted the effective mobility for the short channel devices by using the recently proposed method that uses resistance slope and inversion charge slope with L_{mask} [8].

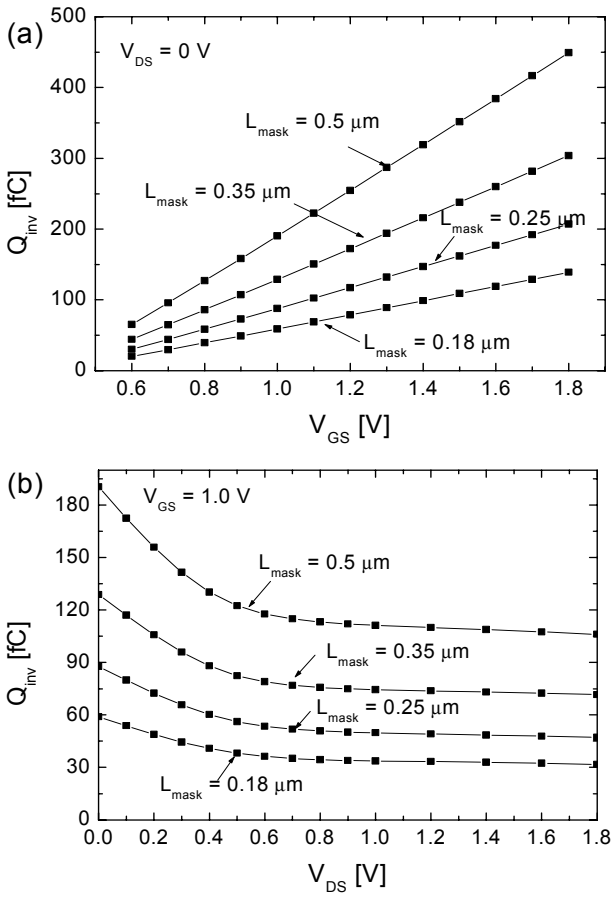

Fig.4. Total inversion charge as a function of gate (a) and drain biases (b). The inversion charge was obtained by integrating the channel capacitances.

Finally, we should measure the total inversion charge. Unfortunately, it is not easy to measure gate-channel capacitances, which are needed to obtain Q_{inv}, in short-channel MOSFETs using conventional low frequency *CV* measurements since the magnitude of the capacitances is very small. Thus, *S*-parameter measurements were used to obtain the accurate *CV* characteristics in short-channel devices. The intrinsic gate-channel capacitances, which are obtained by subtracting bias dependent parasitic capacitance from the measured total capacitance, were path-integrated numerically to obtain total inversion charge. Fig. 4 shows the obtained inversion charge as a function of V_{GS} (a) and V_{DS} (b).

C. Noise Deembedding

To extract the intrinsic drain thermal noise current accurately, the effects of probing pad, interconnection series resistance, gate electrode resistance, source/drain resistance, source/drain junction capacitance, and substrate resistance were extracted and deembedded by using noise correlation method. The effect of parasitic resistances on the extraction of the intrinsic drain thermal noise is shown in the Fig.5. $<i_{ext}^2>$ and $<i_{int}^2>$ represent the measured noise and the intrinsic drain thermal noise of MOSFET, respectively as shown in the inset of Fig.5(a). The source and drain resistances have important effects on the determination of intrinsic channel noise in linear region as shown in Fig.5 (a), where MOSFET can be thought

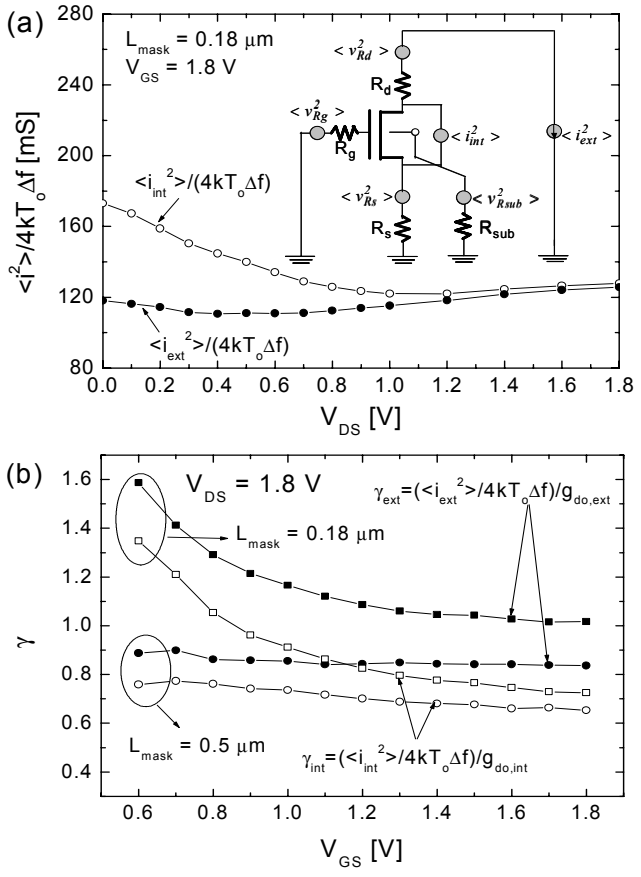

Fig.5. Source/drain resistance has much influence on the determination of intrinsic channel noise in the linear region (a). The change of γ due to the parasitic resistances in the saturation region (b).

as simple resistor, since the impedance of source/drain resistances is comparable to that of intrinsic channel of short channel device biased at the high gate voltage. But at saturation region, $<i_{ext}^2>$ is approximately given by

$$<i_{ext}^2>/4kT_o\Delta f \approx \frac{<i_{int}^2>/4kT_o\Delta f + g_m^2R_s + g_m^2R_g + g_{mb}^2R_{sub}}{(1+F)^2} \quad (2)$$

, where feedback factor $F = (g_m+g_{mb})R_s$.

Equation (2) means that the noises due to parasitic and intrinsic part are less propagated into the extrinsic terminal by the amount of feedback factor in the saturation region. After inserting the ac parameter values of the devices with L_{mask} = 0.18 μm at V_{GS} = 1.8 V into (2), we found $<i_{int}^2> \approx <i_{ext}^2>$ at saturation as shown in Fig.5(a). Often intrinsic drain thermal noise, $<i_{int}^2>$, is expressed as $4kT_o\Delta f \cdot \gamma \cdot g_{do}$--(3)[1], where g_{do} is drain conductance at $V_{DS} = 0$ *V*. For long channel MOSFETs, γ satisfies the inequality $3/2 \le \gamma \le 1$. The value of 2/3 holds when the MOSFET is in the saturation region and the value of one holds when the drain bias is zero. The γ represents the ratio of the value of thermal noise at any given drain bias to the value of thermal noise at V_{DS} = 0 V for the same V_{GS}. Fig.5(b) shows the extrinsic and intrinsic γ for the devices with L_{mask} = 0.18 and 0.5 μm at the saturation region, which indicates that the deembedding of parasitic resistances is important for the determination of γ.

D. Modeling of Drain Thermal Noise

Fig. 6 compares the measured and modeled $<i_{int}^2>$ with (1) as a function of drain bias at V_{GS} = 1.8 V (a) and V_{GS} = 0.6 V (b). The symbol represents the extracted intrinsic drain thermal noise and the solid line represent the modeled value using (1), respectively. The thermal noise decreases steadily until $V_{DS} = V_{DSsat}$, where V_{DSsat} is the drain saturation voltage. In linear region, the model excellently explains the drain bias dependency and channel length dependency of thermal noise for various gate biases. Note that the excellent agreement between the measured and the modeled values at V_{DS} = 0 V, which shows the accuracy of noise measurement and the validity of extracted parameters in section A. Excellent agreements in the linear region indicate that the model properly takes into account the noise behavior for short-channel MOSFET. No large excess noise was observed in contrary to the previous results. And for the high gate voltage of 1.8 V, the thermal noise for all channel lengths stays nearly constant at saturation region, too. However, the moderate increase of drain thermal noise was observed in case of the low gate voltage of 0.6 V and it increased as the channel length was scaled down. We believe that channel length modulation is responsible for this soft increase [9]. The ΔL was obtained with independent *IV* measurement. When ΔL was taken into account in (1), excellent agreement was achieved as shown in the Fig.6 in saturation region, which verifies that excess noise generated in velocity saturation region is negligible. If the total effective channel length (L_{eff}) is used instead of *L* in (1), which is designated in dash-line in the Fig.6, the noise is predicted to decrease beyond the onset of saturation, because the inversion charge is reduced due to CLM effect. Such decrease of the total inversion charge beyond the onset of saturation was still

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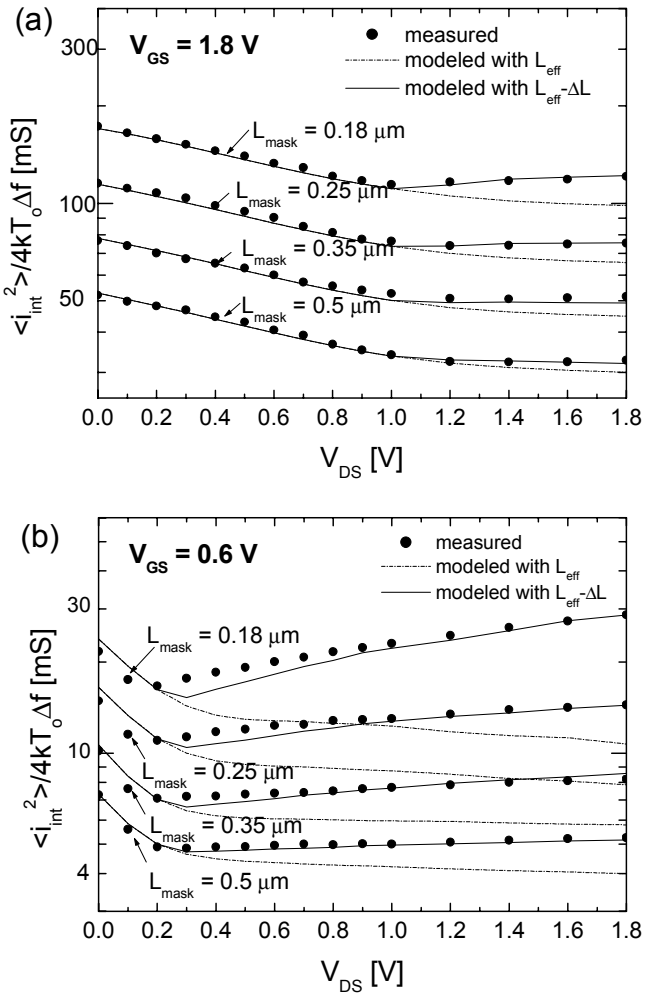

Fig.6. The extracted (symbol) and modeled (solid line: with CLM, dash line: w/o CLM) drain thermal noise vs. V_{DS} at the gate voltage of 1.8 V (a) and 0.6 V (b). Excellent agreement in the linear region indicates that the noise behaviors for short channel MOSFET are described well with the model. Any large excess noise was not observed in saturation region.

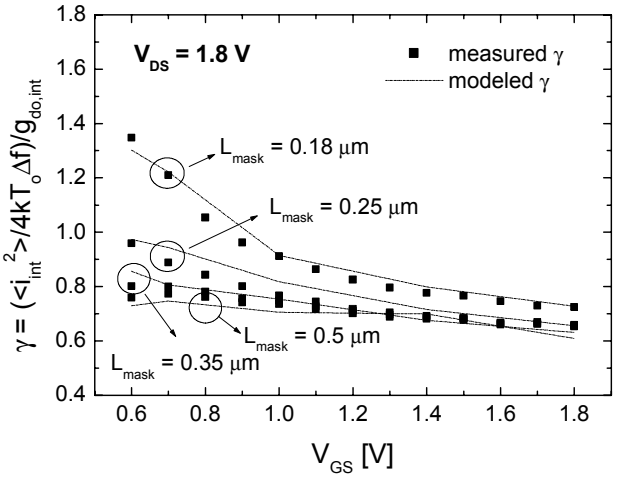

Fig.7. The extracted (symbol) and modeled γ vs. V_{GS} at the drain voltage of 1.8 V. At high gate voltage, γ values for different channel lengths approach to long-channel limit. However, γ increases softly as V_{GS} reaches to V_{TH} due to channel length modulation effect.

observed at V_{GS} = 0.6 V for the device with L_{mask} = 0.18 μm, which means that the static feedback effect is small up to this bias condition. Fig. 7 shows extracted and modeled γ value as a function of gate bias with V_{DS} = 1.8 *V*. γ values for various channel lengths at high gate voltages converge to long-channel limit (γ = *2/3)*. The devices with L_{mask} ≥0.35 μm have showed almost constant γ for varying V_{GS}. In case of devices with L_{mask} < 0.35 μm, γ is bias dependent and increases as V_{GS} approaches to V_{TH}. Such increases of γ value at low gate bias should be understood with increased channel conductance due to the channel length modulation effect.

IV. Conclusion

In this work, the physics-based drain thermal noise model valid for all channel lengths was presented and verified with the measured thermal noise for short-channel nMOSFETs. The accuracies of our noise measurement were checked by measuring the noise at V_{DS} = 0 V. The thermal noise was measured not only in saturation region, but also in linear region. The dependencies of drain thermal noise on channel length, drain and gate biases were explained successfully with the model. The fact that the noise was proportional to large signal quantity, Q_{inv}/L^2, in the entire bias range was shown experimentally for the first time by measuring noise and inversion charge. In contrary to earlier reported large enhancement of thermal noise, no contribution of hot carriers in the velocity saturation region was observed.

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References

[1] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[2] A. A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," *IEEE Trans. Electron Devices*, vol. 33, pp. 1801-1805, November 1986.

[3] A. J. Scholten et.al, "Accurate Thermal Noise Model for Deep-Submicron CMOS," in IEDM *Tech. Dig.*, 1999, pp. 155-1158.

[4] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, New York: McGraw-Hill, 1987.

[5] G. Baccarani and M. R. Wordeman, "An investigation of steady-state velocity overshoot in Silicon," *Solid State Electronics*, vol. 28, no. 4, pp. 407-416, 1985.

[6] Kwangseok Han, Hyungcheol Shin, and Kwyro Lee, "Analytical MOSFET Drain Thermal Noise Current Model Valid for All Channel Lengths," unpublished

[7] K. Takeuchi, N. Kasai, T. Kunio, and K. Terada, "An Effective Channel Length Determination Method for LDD MOSFET's, " *IEEE Trans. Electron Devices*, vol. 43, pp.580-587, April 1996.

[8] S. Lee and H. K. Yu, "A New Technique to Extract Channel Mobility in Submicron MOSFETs Using Inversion Charge Slope Obtained form Measured S-Parameters," *IEEE Trans. Electron Devices*, vol. 48, pp.784-788, April 2001.

[9] M. J. Deen and C.-H. Chen, "MOSFET Modeling for Low Noise, RF Circuit Design," *Proc. Custom Integrated Circuits Conference*, 2002, pp. 201-208.

