Analysis of gate currents through High-K dielectrics using a Monte Carlo Device Simulator

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***Abstract*—The gate current through high-K dielectrics has been calculated by a Monte Carlo simulator. In high-K dielectrics, the gate current from the drain edge is dominant and is quite serious due to a lowering of the barrier height with an increasing dielectric constant. The stack structure of high-K dielectric and oxide films is effective to suppress gate current densities generated from high-energy carriers generated near the drain edge.**

Keywords-component; Monte Carlo, device simulation, high-K, gate current

I. INTRODUCTION

Recently, MOSFETs using high-K gate material are being enthusiastically investigated to suppress the gate current. The suppression of the gate current is a critical issue not only on the power consumption at Vg = 0, but also on the reliability problem at Vg = Vdd. Furthermore, in the case of low stand-by power transistors, the allowable leakage current densities are limited by battery life at any gate bias condition. Near the drain edge, the population of the high-energy electrons increases with the decreasing channel length of MOSFETs. It is known that the injection probability increases with electron energy, and the barrier height generally decreases with the increasing dielectric constant. Also, the rate of injection into the dielectric increases with the decreasing barrier height [1][2].

In a previous study [3], the gate currents through high-K stacks were calculated using W.K.B. method and the decrease of the gate current and the necessity of the barrier height of high-K material greater than applied voltage and fabricated with a few atomic layer of SiO_2 at the interface were shown. Also, in another study [4], it was shown that 'to take full advantage of using high-K dielectrics as gate insulators the residual oxide needs to be eliminated,' when the gate voltage is below the barrier height of dielectrics. But if the population of electron energy near the drain edge under transistor operation is considered, their suggestion might be modified.

In our preliminary study [5], the gate current from the drain edge through high-K dielectrics has been discussed as a function of the electron temperature. In this paper, the gate currents through high-K dielectrics under transistor operation are studied using a Monte Carlo simulator, for the first time. With high-K alone for gate dielectric, serious increases of the gate currents are observed due to the lowering of the barrier height with an increasing dielectric constant. The stack structures with high-K dielectric and oxide films suppress such anomalous high gate currents.

II. SIMULATION MODELS AND EXAMPLES

The calculated (2-dimensional) structure and profile with a n-poly Si gate are shown in Figure 1 where Lg is 45 nm and Tox is 1.2 nm, formed by a 3-dimensional process simulator, HySyProS, a part of our in-house TCAD system called ENEXSS [6]. The structures with Lg 70/100 nm are also calculated as a reference. The calculated Id-Vg characteristics are shown in Figure 2.

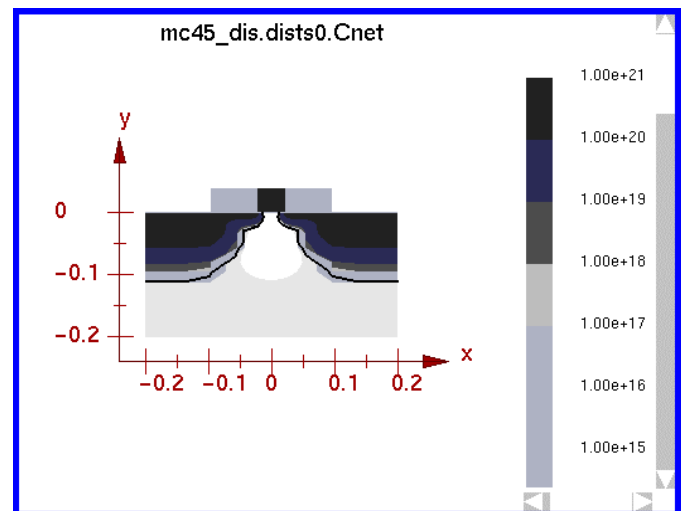

Figure 1. Calculated structure and its impurity profile using ENEXSS system[6]. Lg 45 nm, and EOT 1.2 nm.

In the simulation, the W.K.B. method is used to calculate the injection probability including direct / Fowler-Nordheim tunneling and thermoionic emission. Assuming one-band parabolic dispersion relation for the conduction band and elastic tunneling process. We calculate the gate current by recording all events when a Monte Carlo carrier hit the silicon-

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dielectric interface, multiplying the injection probability of each carrier. The injection probability in our study is dependent on the electron perpendicular (to the interface) kinetic energy, potential barrier shape, and conduction band effective mass of dielectrics. The details of the derivation of the injection probability are shown in elsewhere [5][7].

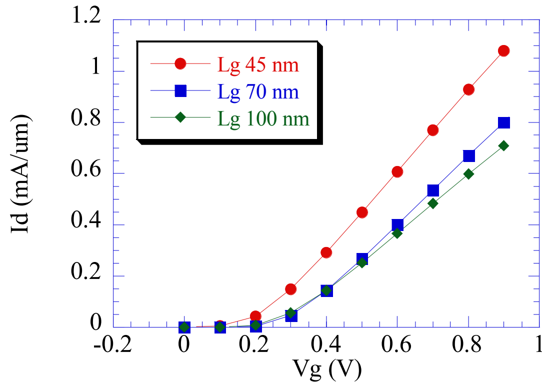

Figure 2. Id-Vg characteristics at Vd = 0.9 V of calculated structures.

As far as the barrier height of high-K is relatively low, and to understand the effect of the barrier height qualitatively, we use non-parabolic model [9], as a full band calculation is time consuming and one-band parabolic dispersion relation is assumed to calculate injection probability. Thus, though we will planning to show the result by a full band calculation in near future, this paper shows the essential and reasonable point of the characteristics of the gate currents under transistor operation. Details of the Monte Carlo simulator used this paper are shown in [8], which contained the standard set of scattering models [9].

In previous studies, the importance of Coulomb interaction have been shown such as "the electron-electron interaction leads to an increase of the high energy tail of the electron distributions at the transition from channel to drain. The electron density around 3 eV is significantly increased even if the applied voltage is in the 1.0 V range," (quoted from [10] as a example,) though they calculated the gates current only through SiO_2, not through high-K stacks. So in this study, Poisson equation is solved self-consistently to include plasmon and carrier-carrier interaction.

To calculate the motion of carriers accurately, the mesh size perpendicular to the interface between silicon and dielectric should be about 0.1 nm or below in this example, because near the interface, the electric field perpendicular to the interface sometimes exceeds 2 MV/cm, i.e. 20 mV per 0.1 nm. Non-uniform rectangular mesh is used and charges were assigned to mesh points using the NGP (nearest grid point) method in the simulation. As the mesh size is small (0.1 nm), the motion of the carriers needed to be updated every 0.1 fs. Poisson equation was solved every 1 fs. Window Monte Carlo technique was also used, and the MC window was set up from 5 nm outside of the source junction to 45 nm out of the drain junction. The drain side of the window is set wider than that of the source due to the distribution of high energy carriers.

III. SIMULATION RESULTS

The typical averaged carrier velocity and energy along the channel are shown in Figure 3. Velocity overshoot is observed in the channel region and the energy is largest near the drain junction. The averaged carrier energy is observed to be still hot in the drain junction.

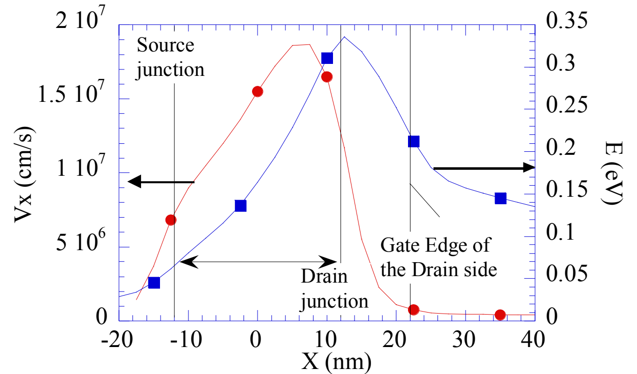

Figure 3. Typical averaged carrier velocity distribution (Vx) and averaged electron kinetic energy distribution (E) distribution along the channel and where Lg = 45 nm and Vd = Vg = 0.9 V.

The typical energy distributions along the channel of the calculated devices are shown in Figure 4. As shown in the Figure 4, the increase of the high energy tail is remarkable at the drain junction and the gate edge of the drain, due to the Coulomb interaction of carriers.

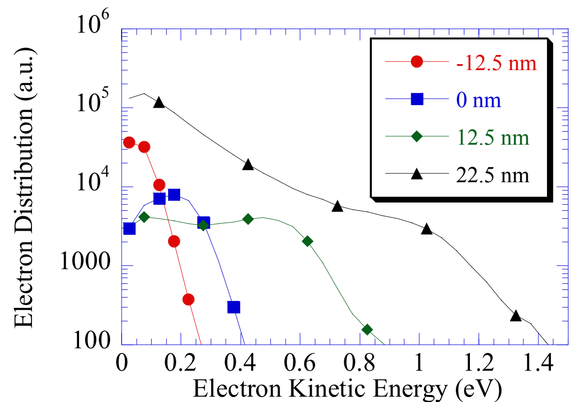

Figure 4. The energy distribution along the channel. The values at the source junction (-12.5 nm), the center of the channel (0 nm), the drain junction (12.5 nm) and the gate edge (22.5 nm) of the drain side are shown. The positions correspond to those in Figure 3.

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The results of the gate currents through SiO_2 and a typical high-K material (assumed to be HfO_2) are shown in Figure 5. The dependence of gate length and the dependence of gate voltage are shown. The parameters used [1] are shown in the caption of Figure 5. The gate currents through high-K are large for a small Lg (Figure 5(a)) value, and show a convex curve on Vg (Figure 5(b)).

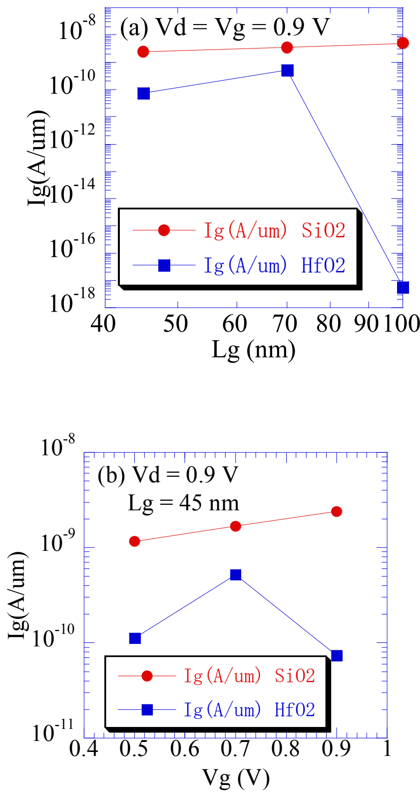

Figure 5. The gate currents through SiO_2 and high-K materials with the same EOT. (a) Lg dependence at Vg = Vd = 0.9 V and (b) Vg dependence at Vd = 0.9 V and Lg = 45 nm. Parameters used to calculate the injection probability are for SiO_2 (dielectric constant ε; 3.9, barrier height χ; 4.1 eV, relative effective mass m*; 0.41 m_0) and for high-K dielectric (ε; 23.4, χ; 2.1 eV [1], m*; 0.2 m_0 [12]).

To explain this dependence of gate currents through high-K, the distribution of the generated gate current densities along the channel is shown in Figure 6. In the case of SiO_2, the values are largest under the source diffusion layer, which means the values essentially depend on the voltage difference between the channel. On the other hand, in the case of high-K, the values are largest under the drain diffusion layer which means the values depend on numbers of high-energy carriers, that is to say, the values depend on the distribution of the lateral electric field along the channel like well known Vg and Lg dependences of the substrate currents.

Note in Figure 5(a), gate currents at Lg = 45 nm are less than that at Lg = 70 nm at Vg = 0.9 V as the lateral electric field near the drain junction is relaxed due to the threshold voltage lowering (the short channel effect) as shown in Figure 2. Also, as far as the gate current through high-K dielectric depend on the distribution of the lateral electric field, so it can suppress by device optimization. The calculated structure in this study was not so optimized, but was fabricated by a typical process condition.

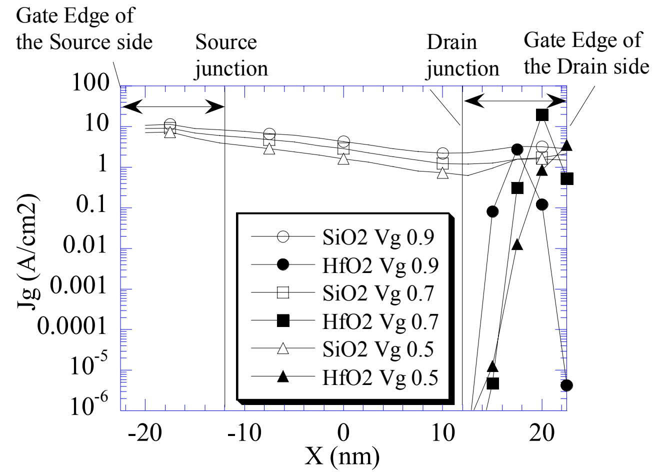

Figure 6. The distribution of the generated gate current density (Jg) along the channel at Vd = 0.9 V and Lg = 45 nm.

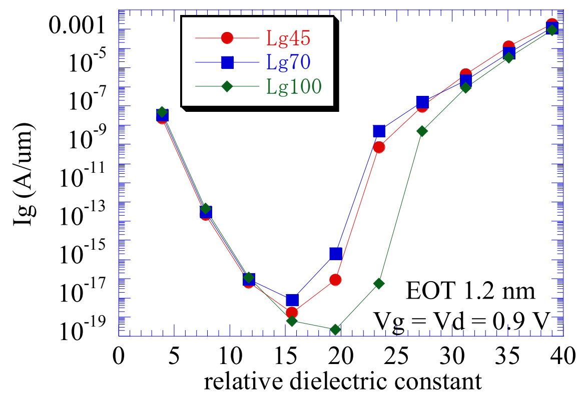

Figure 7. The dielectric constant dependences of the injection current at Vg = Vd = 0.9 V, when the barrier height χ and effective mass m* decreases monotonically with the increase of the dielectric constant. ($\chi = 4.1 - 0.4 (\varepsilon - \varepsilon_{ox}) / \varepsilon_{ox}$ (eV))

The dielectric constant (K value) dependences of the calculated gate currents with different gate lengths are shown in Figure 7. We assumed that the barrier height and effective mass decreases monotonically with the increase of the K value. From the results of [1] and [2], we think this assumption is no less realistic. As shown in Figure 7, in relatively low K values (less than 10), the gate currents decrease with the K value, due to the increase of the dielectric thickness. Also for relatively

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high K values (more than 25), the gate currents increase along with the K value. In medium K values (10-25), the gate currents depend on Lg, which means the gate currents depend on the energy distribution near the drain junction, and become larger than those through SiO_2.

The stack gate structure with high-K dielectric and oxide can be a good choice in order to suppress the gate current since the higher barrier height of oxide prevents injection of high-energy electrons. In Figure 8, the ratio dependences of the high-K dielectric in the gate stack structure on the gate currents with the same EOT (1.2 nm) are shown. The left side of the figure (high-K ratio = 0) represents pure SiO_2, while the right side (high-K ratio = 1) represents a pure high-K dielectric. The gate current at first decreases with the high-K ratio due to the increase of the stack thickness, but in a small Lg, the gate current begins to rise for increasing higher ratio values due to the increase of the high-energy electrons.

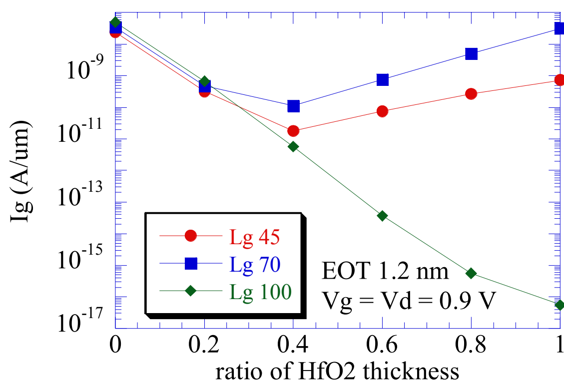

Figure 8. The ratio dependences of high-K dielectric in the gate stack structure on the gate currents through the dielectric stack at Vg = Vd = 0.9 V.

In measurements, a few atomic layer of native oxide would remain essentially between silicon and high-K dielectric. From our results, this oxide would suppress the gate current in measurements. Thus, Figure 8 shows that the gate current can suppress by using a stack structure even if the barrier height of high-K dielectric is relative low, which is consistent with many experimental data, and thus shows the necessity of some thickness of SiO_2 under a high-K dielectric in a stack to suppress the gate current near the drain edge.

Also in the future device (45 nm node and below), the effective oxide thickness will be less than 1 nm, by International Technology Roadmap for Semiconductors (ITRS) 2001 edition [11], so the oxide thickness will need to shrink to be very thin, less than the native oxide thickness. Thus the increase of gate current due to the low barrier height of high-K dielectric under transistor operation will be a serious problem.

IV. CONCLUSION

The gate current through high-K dielectrics has been calculated by a Monte Carlo simulator using the W.K.B method. In short channel devices, the gate current from the drain edge is dominant and is quite serious in high-K dielectrics due to a lowering of the barrier height with an increasing dielectric constant due to the increase of the carriers near the barrier height of high-K dielectrics. The stack structure of high-K dielectric and oxide films is effective to suppress gate current densities generated from high-energy carriers generated near the drain edge.

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