Topography and Schottky Contact Models applied to NiSi SALICIDE Process

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***Abstract*— Nickel monosilicide (NiSi) is considered to be a promising candidate for the self-aligned silicide (SALICIDE) material of 65 nm node MOSFETs and beyond. Therefore, an accurate simulation method for NiSi SALICIDE process is required in order to design the optimum device. We realize, for the first time, the integrated simulation with silicide topography and Schottky contact models, and propose the calibration strategy of contact resistance. In this paper, we demonstrate the accurate simulation results of the silicide both in terms of its topography and contact resistance for NiSi SALICIDE process.**

Keywords-component; NiSi, SALICIDE, topography, Schottky, contact resistance

I. INTRODUCTION

Nickel monosilicide (NiSi) is indispensable for fabricating MOSFET devices, because it consumes less silicon and is formed at lower process temperature than other silicide films such as $TiSi_2$ and $CoSi_2$ [1,2]. Also, it is well known that contact resistance (*Rc*) between silicide and diffusion region is one of the most important device characteristics when the self-aligned silicide (SALICIDE) process is utilized [3]. Therefore, future device technology requires the device simulation with *Rc* using Schottky contact model as well as the process simulation with topography model of NiSi.

Many researchers have reported the simulation results of device characteristics with *Rc* [4]. Oldiges et al. reported a detailed simulation and analysis of the source/drain resistance by using several simulation models such as Schottky contact model. Their report contained significant information for designing diffusion layer, but silicide topography was simplified as box-like region. In order to perform more detailed analysis, it is necessary to simulate the realistic topography of silicide. We realized the integrated simulation with silicide topography and Schottky contact models, and proposed its *Rc* calibration method, especially nickel silicidation. In this paper, we present an accurate and practical simulation method for NiSi SALICIDE process.

In the following section, we describe the content of the simulation method composed of topography model, Schottky contact model and calibration strategy of *Rc*. In section III, we present the simulation results of NiSi topography and *Rc*. Also, we show the relationship between *Rc* and active concentration in the case of nickel silicidation.

II. SIMULATION METHOD

A. Topography simulation

Topography simulation model for the growth of $TiSi_2$ and $CoSi_2$ has been reported [5]. This model is based on the concept of oxidation simulation. We apply this model to nickel silicidation in this work. Figure 1 schematically illustrates the growth mechanism of NiSi. NiSi is formed by reaction of Ni and Si at the interface between NiSi and silicon substrate, and Ni films shrink during the growth of NiSi simultaneously. At this time, Ni atoms are the dominant moving species. The reaction is as follows.

$$\underset{(1)}{Ni} + \underset{(1.84)}{Si} \rightarrow \underset{(2.22)}{NiSi} \qquad (1)$$

In this equation, numbers in parentheses show the volumetric changes [6].

Taking into account the above feature, we solve the diffusion equation of Ni atoms in NiSi. Next, we assume the linear reaction of Ni and Si at the interface between NiSi and silicon substrate. Then, we calculate the displacement velocity

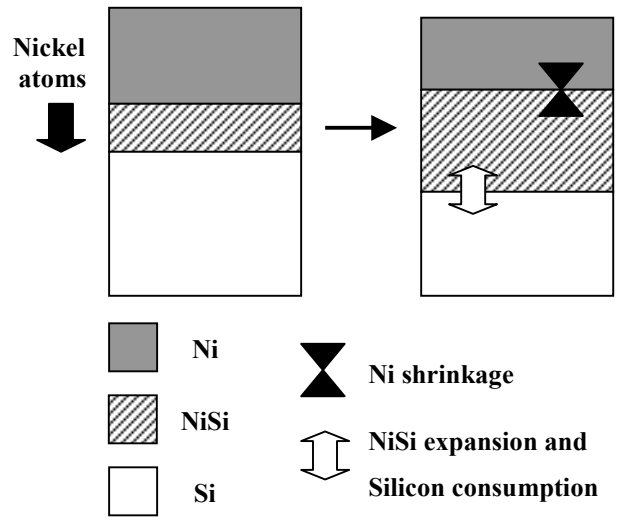


Figure 1. Schematic illustration of the growth mechanism during nickel silicidation.

for the growth of NiSi and the shrinkage of Ni films by solving the viscoelastic model.

B. Schottky contact model

There are several models for calculating the contact resistance [4]. Among these models, Schottky contact model is the most accurate model for reproducing the physical phenomena. In this work, we adopt Schottky contact model that calculates the thermionic emission current and the tunneling current as shown in Fig. 2. In the case of simulating the contact resistance, the tunneling current is the dominant mechanism of current flow, because there is high impurity concentration at the source/drain region of MOSFET devices. This current is determined by the tunneling probability T_{TL} that is formulated as follows.

$$T_{TL}(\xi) = \exp\left(-\frac{4\sqrt{2m^*}(q\phi_B - \xi)^{1.5}}{3\hbar q|E|}\right) \quad (2)$$

where ξ is the carrier energy, q is the electron charge, $\hbar$ is Planck's constant divided by 2π, E is the average electric field, m^* is the effective tunneling mass, and ϕ_B is the barrier height, respectively. The tunneling effective mass and the barrier height are important parameters for calculating the contact resistance. More detailed explanation of this model is described in [7].

C. Calibration strategy of Rc

For making a practical simulation of *Rc*, the calibration strategy is highly significant. Shown in Fig. 3 is the calibration strategy of *Rc* at the interface between NiSi and silicon substrate. First, we calibrate the impurity profile with SIMS data. Next, we determine the active concentration of the impurity by using sheet resistance data without silicide. In both steps, we tune the diffusivity and the cluster model parameters to match the experimental data. Then, the growth of NiSi is calculated by utilizing the topography simulation model shown in (1). This step is inevitable because it determines the active concentration at the interface. Finally,

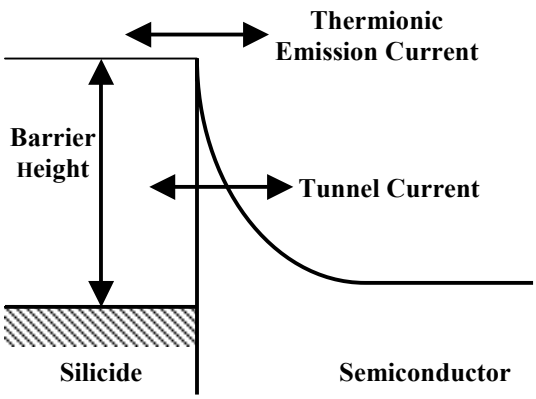


Figure 2. Schematic band diagram at the interface between silicide and semiconductor.

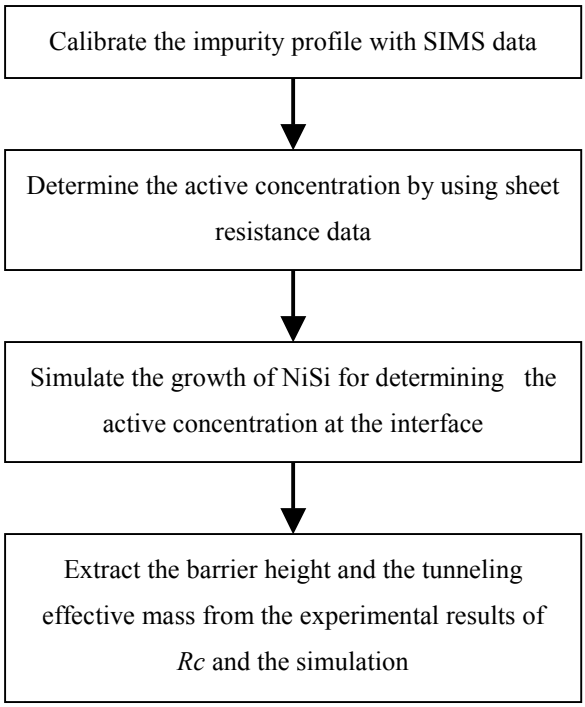


Figure 3. Calibration strategy of the contact resistance at the interface between NiSi and silicon substrate.

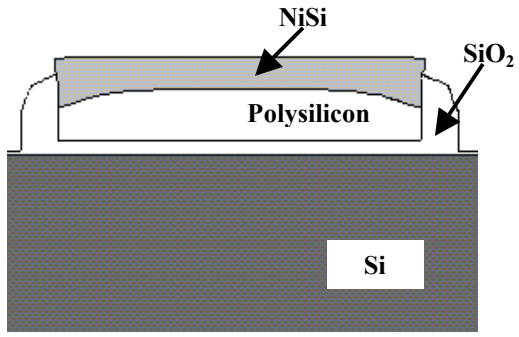
the barrier height and the tunneling effective mass of the Schottky contact model [7] are extracted from the experimental results of *Rc*. *Rc* is calculated by $Rc = R_{sch} - R_{ohm}$, where R_{sch} is obtained by the current-voltage characteristic using the Schottky contact model and R_{ohm} is obtained by that assuming ideal ohmic contact. R_{sch} includes the contact resistance and the intrinsic resistance, whereas R_{ohm} is the intrinsic resistance. And the intrinsic resistance means the resistance of diffusion region and silicide. In this calibration, we assume that there is no deactivation and no diffusion for the impurity during nickel silicidation.

III. SIMULATION RESULTS

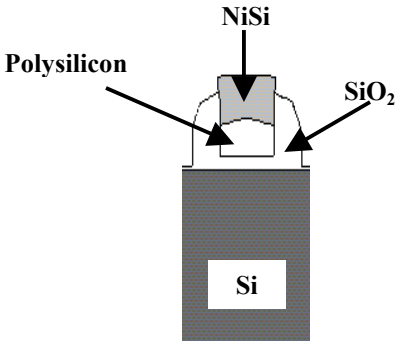
A. Topograpgy simulation of NiSi overgrowth

Figure 4 shows the simulation results of NiSi growth on gate polysilicon. In this calculation, NiSi is formed at 550°C anneal temperature. In the case of long-gate polysilicon, NiSi near the spacer is slightly thicker in Fig. 4(a). In Fig. 4(b), on the other hand, the variation of NiSi thickness is no longer noticeable and the thickness of NiSi at the center of gate polysilicon is slightly thicker for narrow gate polysilicon. This reason is the over-etching of sidewall spacer, that is, the reduced spacer exposes partial gate polysilicon sidewall to Ni films and results in a thicker NiSi. Both results are in good agreement with the TEM images [8].

The relationship between the effective thickness of NiSi and gate polysilicon length is shown in Fig. 5. The effective thickness means the thickness of NiSi at the center of gate



(a)



(b)

Figure 4. Simulation results of NiSi growth on gate polysilicon (a) 1 μm length, (b) 0.2 μm length.

polysilicon. It is shown that the narrower the length of gate polysilicon, the thicker the effective thickness of NiSi. In the case of 50 nm gate polysilicon, the effective thickness is about twice that of the long-gate polysilicon. This result corresponds to Xiang's report [9]. These results show that it is possible to simulate the topography of NiSi accurately.

B. Rc simulation with Schottky contact model

We investigated *Rc* for a wide range of source/drain implant conditions. In the present samples, the implanted dopant was activated by spike anneal. After the Ni films deposition, NiSi SALICIDE process was carried out at 450°C anneal temperature. The contact resistance at the interface between NiSi and silicon substrate was measured by Kelvin pattern at room temperature. In the measured *Rc*, the parasitic resistance such as sheet resistance of NiSi and diffusion region was included. Therefore, we eliminated the parasitic resistance by means of 3-D device simulation.

Shown in Fig. 6 is the contour plot for *Rc* in n^+Si when the barrier height is 0.67eV. We extracted a unique value of the tunneling effective mass from this figure by utilizing the calibration strategy described in section II-C. Also, we determined that for hole in the same scenario. Figures 7 and 8

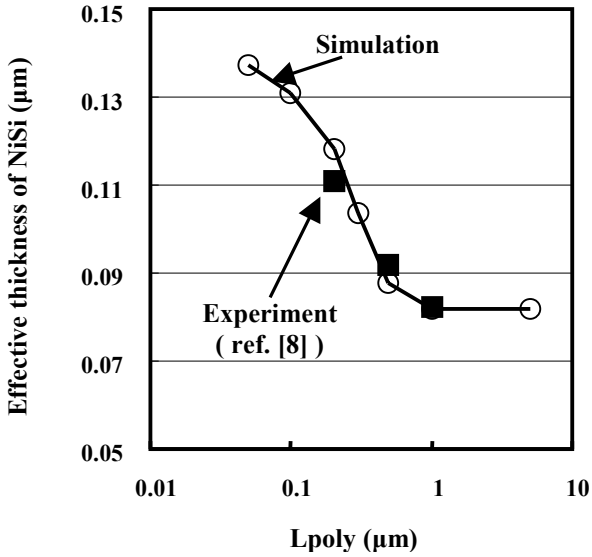


Figure 5. Effective thickness of NiSi versus gate polysilicon length. Open circles are simulation results, solid squares are experimental data [8].

show the comparison of simulation results and experimental data of *Rc* for NiSi/ phosphorus-doped n^+Si and NiSi/ boron-doped p^+Si, respectively. In these figures, our simulation reproduces measured results quite well.

It is well known that active concentration at the silicide interface is an important parameter for *Rc* as well as the barrier height and the tunneling effective mass. Shown in Fig. 9 are the simulation results of *Rc* for active concentration at the interface between NiSi and silicon substrate. In this figure, it is found that *Rc* of p^+Si is lower than that of n^+Si at the same active concentration. This is a merit of NiSi that is utilized for the contact material of source/drain region. Because, it is well

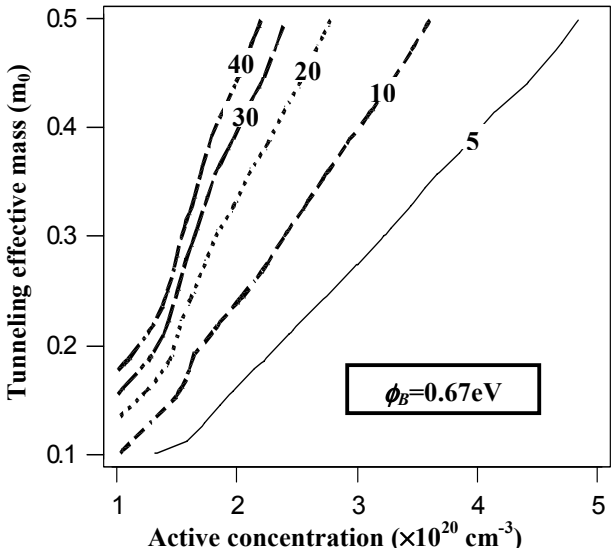


Figure 6. Contour plot for the contact resistance in n^+Si. The unit of the contact resistance is $\Omega\mu m^2$.

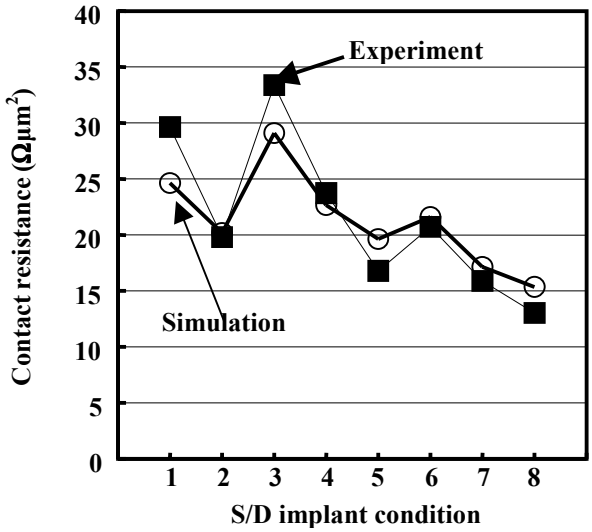


Figure 7. The contact resistance for NiSi/ n^+Si. Open circles are simulation results, solid squares are experimental data.

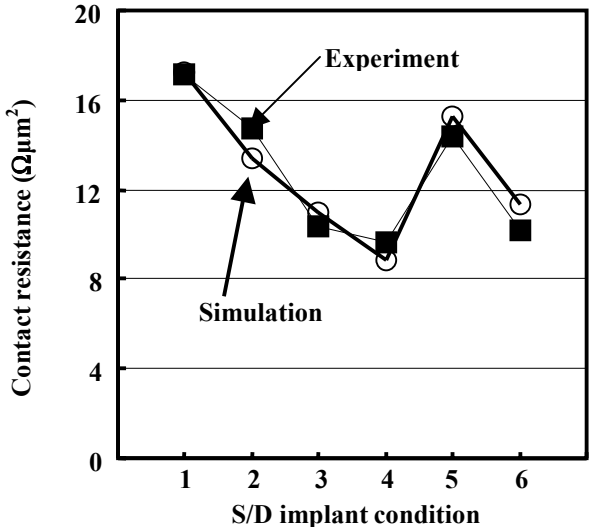


Figure 8. The contact resistance for NiSi/ p^+Si. Open circles are simulation results, solid squares are experimental data.

known that activation rate of dopant in n^+Si is higher than that of dopant in p^+Si at the same anneal temperature. Therefore, making use of NiSi, both nMOSFET and pMOSFET could be fabricated with low contact resistance. Our simulation shows that it is necessary to activate about 7×10^{20}cm^{-3} for n^+Si and about 3×10^{20}cm^{-3} for p^+Si, if *Rc* is less than 2 Ωμm^2 for future device fabrication.

IV. CONCLUSION

We presented an integrated simulation method with silicide topography and Schottky contact models, and its calibration strategy for *Rc*. Using the present simulation method, accurate simulation of the silicide both in terms of its topography and *Rc* for NiSi SALICIDE process can be performed. Furthermore, we extracted the relationship between *Rc* and active concentration as shown in Fig. 9. This simulation method is expected to serve a wide range of applications in future device development.

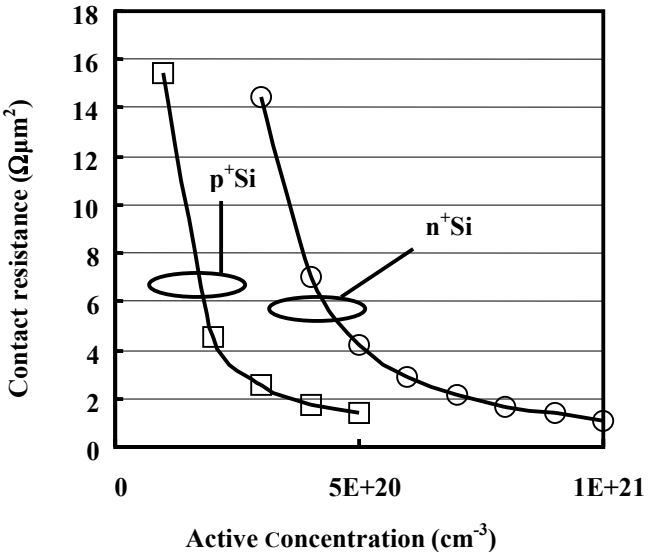


Figure 9. Simulation results of the contact resistance for active concentration at the NiSi/ Si interface.

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