A Novel Technique for Full-wave Modeling of Large-scale Three-dimensional High-speed On/Off-chip Interconnect Structures

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***Abstract*—This paper presents a novel, rigorous, and fast method for full-wave modeling of high-speed interconnect structures. In this method, the original wave propagation problem is represented into a generalized eigenvalue problem. The resulting eigenvalue representation can comprehend conductor and dielectric losses, arbitrary dielectric and conductor configurations, and arbitrary materials such as dispersive, and anisotropic media. The edge basis function is employed to accurately represent the unknown field, and the triangular element is adopted to flexibly model arbitrary geometry. A mode-matching technique applicable to lossy system is developed to solve large-scale 3D problems by using 2D-like CPU time and memory. A circuit-based extraction technique is developed to obtain S-parameters from the unknown fields. The proposed technique can generate S-parameters, full-wave RLGC, propagation constants, characteristic impedances, voltage, current, and field distributions, and hence yield a comprehensive representation of interconnect structures. Experimental and numerical results demonstrate its accuracy and efficiency.**

Keywords-high-speed interconnect; on/off-chip; full-wave modeling

I. INTRODUCTION

As the clock frequency of microprocessors enters the giga-hertz regime and heads towards 20GHz level, accurate full-wave modeling of on- and off-chip interconnect structures is becoming increasingly important. In recent years, a variety of full-wave modeling techniques, such as the finite-difference time-domain (FDTD) method [1-4], the integral equation based methods [5-7], and the finite element method (FEM) [8-9] have been applied to the simulation of high-speed interconnects. Although they have gained extensive application for board- and package-level interconnect problems, little work has been reported on the full-wave analysis of on-chip interconnect structures.

On-chip interconnect structures present many challenges that are less pronounced in board and package level interconnects such as high loss, large aspect ratio, large number of conductors, and strong non-uniformity in dielectric stack. These challenges result in large computational complexity and prevent the direct use of existing full-wave techniques. For instance, FDTD usually requires a time step that is constrained by the smallest spatial step to ensure stability. This hinders its application to realistic on-chip problems since on-chip interconnects feature geometries ranging from less than 0.1 micron to thousands of microns. Although this problem can be eliminated by developing an unconditionally stable FDTD scheme [4], the computation remains expensive due to the large number of unknowns resulting from the 3D geometries and the fine discretization required to capture skin effects. Full-wave based integral-equation methods generally break down at the low frequencies that lie within the frequency band of on-chip interconnects [11]. Although advanced numerical techniques [11] can be utilized to eliminate this issue, other shortcomings limit its usefulness. The method itself either can only be applied to the cases wherein the Green's function is available (surface integral equation based methods), or has to be formulated into a computationally intensive volume integral equation so that the complicated inhomogeneity can be modeled. As far as the finite element method is concerned, although it can efficiently comprehend arbitrary inhomogeneity, most existing solvers neglect the intricacies of on-chip interconnects or introduce approximate models to simplify the problem, and hence fail to capture the on-chip physical phenomena satisfactorily without further development.

In this paper, we propose a novel, fast and accurate full-wave modeling technique that is applicable to both on- and off-chip interconnect structures. In this technique, the complexity of 3D interconnects is overcome by seeking the full-wave solution of a few 2D problems, which are then post-processed to obtain the solution of the original 3D problem. The entire procedure is rigorous, and does not introduce approximations. This methodology provides an accurate solution to 3D interconnect problems by only employing 2D-like CPU time and memory. Experimental and numerical results demonstrate the accuracy and efficiency of the proposed modeling technique.

II. FORMULATION

To model 3D interconnect structures, first we identify a set of unique structure seeds. Take a typical Manhattan-type interconnect shown in Fig. 1 as an example, the number of unique structure seeds is only 8 although the structure itself can consist of thousands of segments (a segment has a constant cross section). If we use three digits to describe each structure

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seed, the 8 structure seeds can be represented by 000, 001, …, 111 respectively. The first, second, and third digits correspond to M5, M3, and M1 layers respectively. For each digit, value 0 denotes the absence of the orthogonal lines in that layer, whereas value 1 denotes its presence. If the orthogonal lines are aligned in each layer, the total number of unique structure seeds is only 2. One refers to the presence of all of the orthogonal conductors. The other denotes their absence. The structure seeds are repeated along the longitudinal direction, constructing the entire structure.

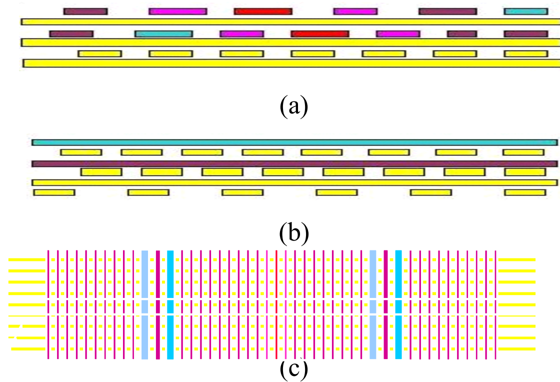

Fig. 1 Geometry of a 3D interconnect structure (a) End view. (b) Side view. (c) Top view.

Next, we perform full-wave modeling of each structure seed. Here, in contrast to the common practice of analyzing interconnect structures by formulating a deterministic problem; we construct an eigen-value based method. This is in light of the fact that the electrical properties of interconnects are intrinsic in nature irrespective of the excitation.

The electric field E in an interconnect structure satisfies the second-order vector wave equation

$$\nabla\times(\mu_r^{-1}\nabla\times\mathbf{E})-k_0^2\varepsilon_r\mathbf{E}+j\omega\mu_0\sigma\mathbf{E}=0 \quad \text{in } \Omega \qquad (1)$$

subject to certain boundary conditions such as

$$\hat{n}\times\mathbf{E}=0 \qquad \text{on } \Gamma_1$$
$$\hat{n}\times(\nabla\times\mathbf{E})=0 \qquad \text{on } \Gamma_2 \qquad (2)$$

In (1), μ_r, ε_r, and σ denote the relative permeability, relative permittivity, and conductivity respectively. The incorporation of conductivity σ allows for the accurate modeling of both conductor and dielectric loss. This is of great importance for the accurate simulation of on-chip interconnects in which skin effects are dominant, and off-chip ones in which both skin effects and dielectric losses are important. By applying variational principle, it can be demonstrated that solving the boundary-value problem defined by (1) and (2) is equivalent to seeking the stationary point of the following functional [10]

$$F(\mathbf{E})=\frac{1}{2}\iint_\Omega[\mu_r^{-1}(\nabla\times\mathbf{E})\cdot(\nabla\times\mathbf{E})-k_0^2\bar{\varepsilon}_r\mathbf{E}\cdot\mathbf{E}]d\Omega \qquad (3)$$

where ε_r with over-bar refers to the complex relative permittivity which comprises ε_r and σ.

Each structure seed has a constant cross-section, and hence inside of which wave propagating along longitudinal direction is analytical. Therefore, the z-dependence of all field components is $e^{-\gamma z}$. With this, (3) can be rewritten as

$$F(\mathbf{E})=\frac{1}{2}\iint_\Omega[\mu_r^{-1}(\nabla_t\times\mathbf{E}_t)\cdot(\nabla_t\times\mathbf{E}_t)-k_0^2\bar{\varepsilon}_r\mathbf{E}\cdot\mathbf{E}$$
$$+\mu_r^{-1}(\nabla_t E_z+\gamma\mathbf{E}_t)\cdot(\nabla_t E_z+\gamma\mathbf{E}_t)]d\Omega \qquad (4)$$

Where ∇_t denotes the transverse del operator, E_t represents the transverse component of the electric field, and E_z signifies the z-component of the field.

To seek the solution of the above variational problem, the computational domain Ω is subdivided into small triangular elements. The transverse field within each element is expanded as

$$\mathbf{E}_t^e=\sum_{i=1}^{n}e_{ti}^e\mathbf{N}_i^e \qquad (5)$$

where n denotes the number of basis functions per element, and N_i and e_{ti} denote the vector expansion functions, and corresponding expansion coefficients respectively. In this paper, edge basis functions [10] are employed to expand the tangential field. The longitudinal field is represented by node basis functions ς_i

$$E_z^e=\sum_{i=1}^{n}e_{zi}^e\zeta_i^e \qquad (6)$$

in which e_{zi} is the corresponding expansion coefficient. The final discretization of the variational problem (4) results in a generalized eigenvalue problem

$$\begin{bmatrix}\mathbf{A}_{tt} & \mathbf{A}_{tz}\\ \mathbf{A}_{zt} & \mathbf{A}_{zz}\end{bmatrix}\begin{Bmatrix}e_t\\ e_z\end{Bmatrix}=\gamma^2\begin{bmatrix}\mathbf{B}_{tt} & \mathbf{B}_{tz}\\ \mathbf{B}_{zt} & \mathbf{B}_{zz}\end{bmatrix}\begin{Bmatrix}e_t\\ e_z\end{Bmatrix} \qquad (7)$$

in which **A** and **B** are complex matrices. Obviously, the eigenvalues of the above matrix system correspond to the propagation constants, whereas the eigenvectors characterize the transverse and longitudinal fields. Once (7) is solved, the electric field in each structure seed can be obtained as

$$\mathbf{E}=\sum_{m=1}^{n}[\alpha_m\mathbf{e}_m(x,y)e^{-\gamma_m z}+\beta_m\mathbf{e}_m(x,y)e^{\gamma_m z}] \qquad (8)$$

which is a superposition of all of the forward and backward propagation modes that can be supported by the structure. It should be noted that the E field in (8) has all three components E_x, E_y, and E_z.

Finally, we determine the unknown coefficients α_m, β_m by imposing field continuity condition at each junction. As an example, consider the junction in the following figure, which separates regions I and II.

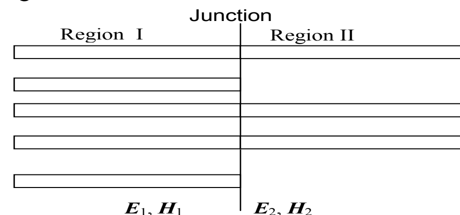

Fig. 2 Illustration of a junction discontinuity in a 3D interconnect structure.

In region I, there are M1, M2, M3, M4, and M5 layers, whereas in region II, only M2, M3, and M5 are present. The electric field in region I can be represented into

$$\mathbf{E}_1=\sum_{m=1}^{M}\xi_{1m}\mathbf{e}_{1m}(x,y) \qquad (9)$$

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in which $\xi_{1m} = \alpha_{1m} e^{-\gamma_{1m} z} + \beta_{1m} e^{\gamma_{1m} z}$, and M denotes the number of modes. Similarly, the electric field in region II can be written as

$$\mathbf{E}_2 = \sum_{m=1}^{N} \xi_{2m} \mathbf{e}_{2m}(x, y) \quad (10)$$

in which $\xi_{2m} = \alpha_{2m} e^{-\gamma_{2m} z} + \beta_{2m} e^{\gamma_{2m} z}$, and N denotes the number of modes in region II. To impose field continuity condition at each junction, we can resort to the mode matching technique [12]. However, the conventional mode matching technique only applies to lossless system. Whereas, interconnect structures especially on-chip interconnects are highly lossy due to the conductor loss and the low working frequency. This problem was solved by developing a novel mode matching technique valid for lossy systems in this paper.

Solution of the fields enables the calculation of circuit parameters. S-parameters and per unit length transmission line parameters are typically of interest to circuit designers. Transmission line description is only valid when quasi-static assumption holds true and the structure is pure 2D in nature. If the structure is 3D in nature, a single transmission line cannot represent its equivalent circuit. In contrast, the S-parameters are always applicable to both low and high frequencies, and 2D/3D structures.

When the transmission line model is valid, the RLGC parameters can be extracted in the following fashion. First, we obtain the eigen-voltage and eigen-current of each conductor for each mode by performing the following line or area integrals

$$\begin{aligned} v_{m,i} &= \int \mathbf{e}_{m,t}(x, y) \cdot dl_i \qquad i = 1, 2, \cdots, n \\ \iota_{m,i} &= \oiint [j\omega\varepsilon e_{m,z}(x, y) + \sigma e_{m,z}(x, y)] dS_i \end{aligned} \quad (11)$$

where m denotes the index of mode; i denotes the index of conductor; $e_{m,t}(x, y)$, and $e_{m,z}(x, y)$ represent the tangential, and longitudinal electric field of the m-th eigen-mode respectively. Substituting (11) and propagation constant γ_m into the telegraph equation:

$$\begin{aligned} \gamma_m \{v_{m,i}\} &= [R + j\omega L]_{i,j} \{\iota_{m,j}\} \\ \gamma_m \{\iota_{m,i}\} &= [G + j\omega C]_{i,j} \{v_{m,j}\} \\ i = 1, 2, \cdots n; \; j &= 1, 2, \cdots n; m = 1, 2, \cdots M \end{aligned} \quad (12)$$

we obtain the RLGC matrices. Note that in contrast to the RLGC matrices obtained via quasi-static solvers that employ a decoupled electric and magnetic field model, here, any coupling between E and H, no matter how weak, is captured accurately.

For 3D interconnect structures or interconnects working at high frequencies, S-parameters become a necessity for an accurate description of their electrical behavior. Two approaches are commonly used in the full-wave area for S-parameter extraction. One is to extract the S-parameters from the standing wave pattern on the feed line; while the other is to obtain the same from the reflected and transmitted fields. Instead of adopting either of these methods, here, we propose a more convenient circuit-based S-parameter extraction technique. Basically, we first construct the total voltage and current of each conductor at the ports of an interconnect by performing the following integrals:

$$\begin{aligned} V_i &= \sum_{m=1}^{M} [(\alpha_m e^{-\gamma_m z} + \beta_m e^{\gamma_m z}) \int \mathbf{e}_{m,t}(x, y) \cdot dl_i] \\ I_i &= \sum_{m=1}^{M} [(\alpha_m e^{-\gamma_m z} - \beta_m e^{\gamma_m z}) \oiint (j\omega\varepsilon e_{m,z} + \sigma e_{m,z}) dS_i] \\ i &= 1, 2, \cdots n; j = 1, 2, \cdots n; m = 1, 2, \cdots M \end{aligned} \quad (13)$$

Then we load each conductor by the reference impedance (usually 50Ω in industry standard), and excite the conductor in turn, which can be mathematically represented as:

$$\begin{cases} V_i + Z_{ref} I_i = 1, & i = 1, 2, \cdots, n \\ V_j + Z_{ref} I_j = 0, & j = 1, 2, \cdots, n, j \neq i \end{cases} \quad (14)$$

The loading condition in (14) together with the boundary condition at each junction yield the solution of unknown coefficients α_m, β_m, and hence the total voltage and current of each conductor. As a result, the S-parameters can be obtained as follows:

$$S_{ij} = \frac{V_j - Z_{ref} I_j}{V_i + Z_{ref} I_i}, \quad i = 1, 2, \cdots, n; j = 1, 2, \cdots n \quad (15)$$

It is worth mentioning that the eigen-system (7) only needs to be solved for each unique structure seed, whose number is many orders of magnitude less than that of the segments. To further speed up the numerical simulation, we also developed a series of acceleration techniques such as fast eigen-value solution, junction matrix acceleration scheme etc. These techniques will be published in the future.

III. NUMERICAL RESULTS

To test the accuracy of the proposed algorithm, we simulated and measured a set of interconnect structures that were fabricated on a test chip using conventional Si processing techniques. Although the test structures involve thousands of conductors, due to the efficiency of the proposed scheme, simulations in the 0-50 GHz range were completed in just minute using a 700MHz Personal Computer. High resolution cross-sectional Scanning Electron Microscopy and Optical Microscopy were used to measure the relevant dimensions of the fabricated structures. Parasitics signals were removed from the measured S-parameters using a de-embedding approach. Figure 3 compares measured and simulated S-parameters of an on-chip interconnect fabricated on a three-metal-layer testchip, and shows an excellent agreement both in magnitude and phase.

Fig. 4(a) compares the simulated and measured crosstalk of an on-chip interconnect. Again, it shows an excellent agreement between experiments and simulations. Fig. 4(b) depicts the current distribution on a sliced cross section at 40GHz with the excited signal on the left in the M2 layer. The current induced on surrounding conductors exhibits a complex pattern, which reflects the mutual coupling among these conductors. In addition, we observe return currents in the lossy silicon substrate. The current nulls observed in the substrate are

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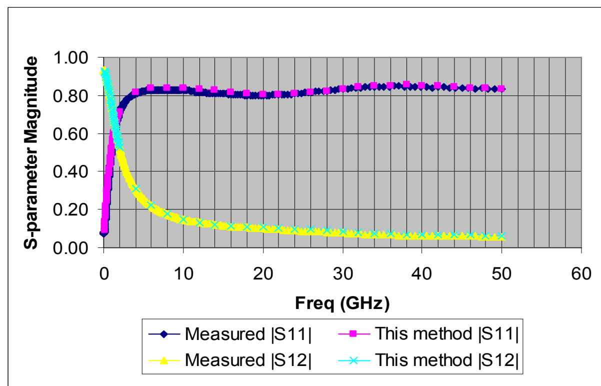
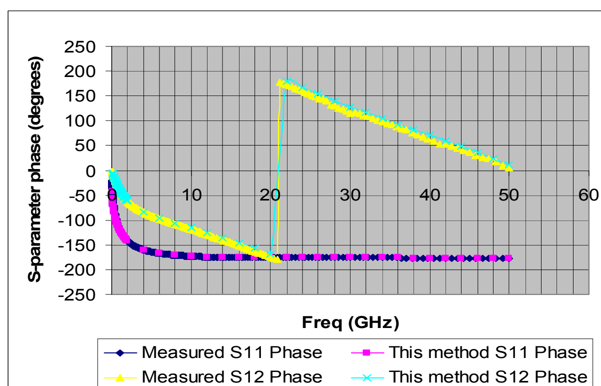
due to the destructive interaction between reflected and transmitted waves.



(a)



(b)

Fig. 3 S-parameters of a 3D on-chip interconnect. (a) Magnitude. (b). Phase.

IV. Conclusion

This paper presents a novel fast full-wave modeling technique for large-scale 3D high-speed on- and off-chip interconnects. This technique formulates a generalized eignvalue formulation of the original wave propagation problem that can comprehend arbitrary dielectric and conductor configurations, both conductor and dielectric losses, and arbitrary materials. A mode matching technique valid for lossy systems is developed to solve large-scale 3D problems with 2D-like computational expenses. A comprehensive characterization of the interconnect is conducted, which includes the extraction of S-parameters, full-wave RLGC, propagation constants, characteristic impedances, voltage, current, and field distributions. Comparison of numerical with experimental results demonstrates its validity. The proposed technique has also been extended to time domain, the detail of which will be reported elsewhere.

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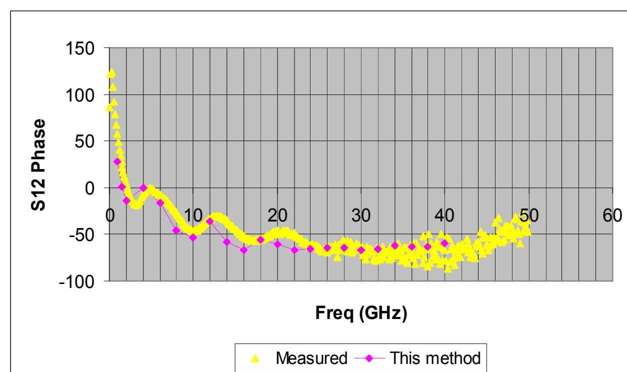
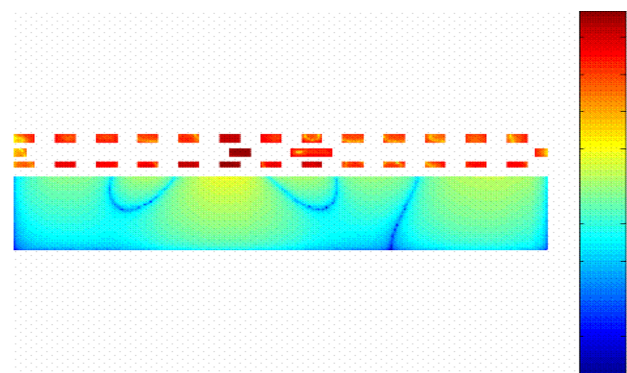


(a)



(b)

Fig. 4 Simulation of a 3D on-chip cross-talk structure (a) Phase of S12 (b) A cross section of the crosstalk structure showing the calculated current distribution.

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