Non-Destructive Inverse Modeling of Copper Interconnect Structure for 90nm Technology Node

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***Abstract*— We propose non-destructive inverse modeling of copper interconnect cross-sectional structure, which reproduces the pitch dependence of intra- and interlayer coupling capacitance parasitic to the interconnect. The coupling capacitances as well as fringing capacitance are measured by proposed test structure based on Charge-Based Capacitance Measurement (CBCM) method [1]. The present methodology not only provides accurate assessment of actual capacitance variation but provides valuable feedback on the variability of physical parameters such as interlayer dielectric (ILD) thickness and interconnect drawn width reduction or swelling for process control as well. It also ensures the accuracy of LPE (Layout Parameters Extraction) for 90nm technology node and beyond.**

I. Introduction

Interconnect delay becomes dominant in total circuit delay especially for 90nm technology node and beyond [2]. Therefore, extraction of interconnect parasitic capacitance for LPE tools determines the accuracy of circuit delay simulation. In addition, the width and height of copper interconnect largely depend on the pitch of the interconnect because fluctuation due to OPC and CMP process is very sensitive to the pitch of the interconnect as well as local layout patterns around the interconnect. Conventional LPE tools, however, assume that width and height of the interconnect are always identical to target specification in spite of their pitch dependence. To cope with this problem, we propose a new CBCM [1] test structure and non-destructive inverse modeling of interconnect structure.

II. Test Structure

Fig. 1 is an explanatory diagram schematically showing a circuit configuration of the proposed test structure measuring the intra- and interlayer coupling capacitance parasitic to copper interconnects, respectively. A PMOS transistor MP and an NMOS transistor MN comprise a charging circuit of CBCM test structure [1]. Employed wave forms of GP and GN are same as those of Ref. 1. Measuring target nodes NA and NB each have a comb-like structure and they are located such that n teeth of the measuring target nodes NA and NB are in opposed spaced relation with predetermined intervals. Transmission gates X, Y and an inverter serve as a terminal state changer, which changes the state of the terminal P2 (node NB) based on selection signal SEL.

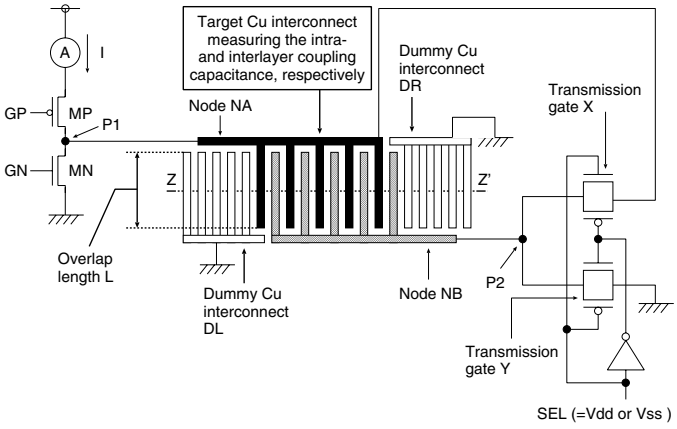

Fig. 1. Schematic of the proposed CBCM test structure measuring the intra- and interlayer capacitance, respectively. SEL represents a selection signal.

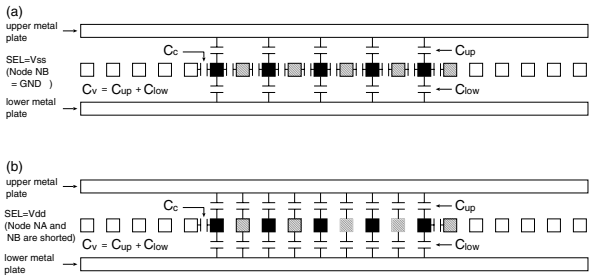

Fig. 2. Cross-sectional view showing cross-sectional configuration taken along line Z-Z′ of Fig. 1 when the selection signal SEL is (a) V_{ss} and (b) V_{dd}. C_c and C_v represent intra- and interlayer coupling capacitance, respectively.

Fig. 2 shows the cross-sectional configuration taken along the line Z-Z′ of Fig. 1. Fig. 2(a) shows the case where the selection signal SEL = V_{ss} and the measuring target node NB is grounded through the transmission gate Y which is in the on-state, while Fig. 2(b) shows the case where the selection signal SEL = V_{dd} and the measuring target nodes NA and NB are short-circuited.

As shown in Fig. 2(a), where the selection signal SEL is V_{ss} (first state), $(2n-1)$ intralayer coupling capacitances C_c (in the example of Fig. 2(a), $n=5$) are formed between respective ones of the teeth of the measuring nodes NA and

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NB and one coupling capacitance C_c is formed between the rightmost teeth of the dummy node DL and the leftmost teeth of the measuring target node NA. Thus, a total of $2n$ coupling capacitances C_c is formed. Further, n interlayer capacitances C_v are formed between the measuring target node NA and an upper interconnect layer MU (C_{up}) as well as between the node NA and a lower interconnect layer ML (C_{low}), i.e., $C_v = C_{up} + C_{low}$. Minor capacitance α refers to parasitic capacitance occurring at connections between the gates of transistors forming the transmission gates X, Y and the inverter and occurring at portions other than the teeth of the target interconnects. Accordingly, a total capacitance $C_{total}(SEL = V_{ss})$ is given by the following equation:

$$C_{total}(SEL = V_{ss}) = (2n \times C_c + n \times C_v) \times L + \alpha \quad (1)$$

where L is the overlap length of the teeth.

As shown in Fig. 2(b), where the selection signal SEL is V_{dd} (second state), since the measuring target nodes NA and NB are short-circuited, only one coupling capacitance C_c is formed between the rightmost teeth of the dummy node DL and the leftmost teeth of the measuring target node NA and only one coupling capacitance C_c is formed between the leftmost teeth of the dummy node DR and the rightmost teeth of the measuring target node NB. That is, a total of two intralayer coupling capacitances C_c is formed. Further, $2n$ interlayer coupling capacitances C_v are formed between the measuring target nodes NA, NB and the upper and lower layer MU, ML. Minor capacitance β is also formed. Accordingly, the total capacitance $C_{total}(SEL = V_{dd})$ is given by

$$C_{total}(SEL = V_{dd}) = (2 \times C_c + 2n \times C_v) \times L + \beta \quad (2)$$

$C_{total}(SEL = V_{ss})$ and $C_{total}(SEL = V_{dd})$ are measured by CBCM technique in two test structures having the different overlap length L. The coupling capacitances C_c and C_v per unit length are obtained by solving four simultaneous equations (1) and (2) for the different overlap length L. The parasitic capacitances α and β are assumed to be same for the CBCM test structures having the different overlap length L; the capacitances parasitic to comb edge of the target layout are completely removed from the target coupling capacitances.

Figs. 3 and 4 show intra- and interlayer coupling capacitances measured by the proposed CBCM test structure in comparison with those given by LPE based on the designed metal 1 and 2 interconnect structures, respectively. The deviation is attributed to the interconnect pitch dependent fluctuation of the OPC and CMP process. Fig. 5 shows the correlation between the measured resistance and coupling capacitance [(a) C_c, (b) C_v] associated with the metal 1 parallel lines between the upper and lower plate, which are fabricated in the same chip. For the purpose of matching the fluctuation due to the OPC and CMP process, interconnect pattern density both in the CBCM and Kelvin TEG pattern is arranged to be same, i.e., approximately 35.2% for a 70μm square window which corresponds to the area for the TEG patterns between two pads located side by side. Strong correlation appears between the resistance and the intralayer coupling capacitance with

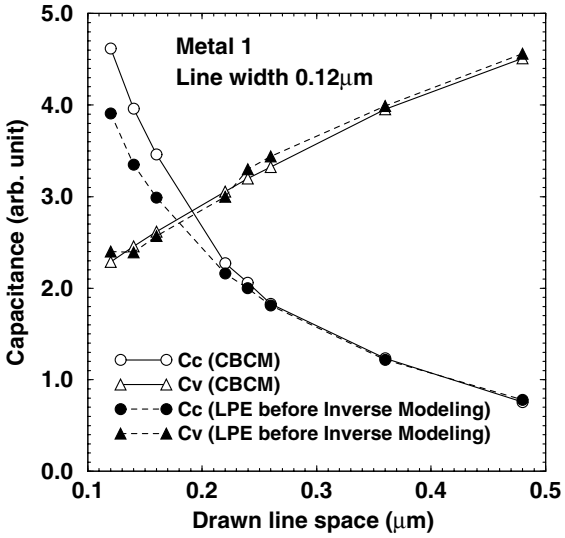

Fig. 3. Drawn line space dependence of intra- and interlayer coupling capacitance in the metal 1 layer (worst case). Drawn line width is 0.12μm.

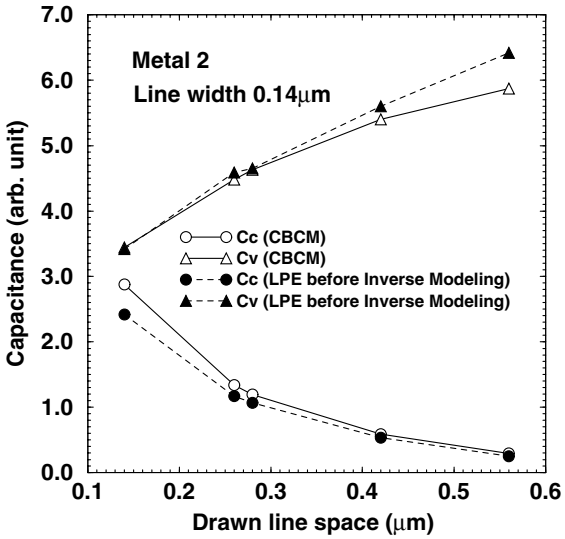

Fig. 4. Drawn line space dependence of intra- and interlayer coupling capacitance in the metal 2 layer (worst case). Drawn line width is 0.14μm.

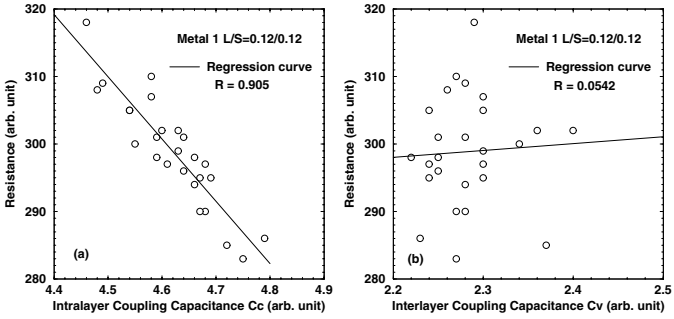

Fig. 5. Correlation between resistance and coupling capacitance [(a) C_c, (b) C_v] in the metal 1 layer fabricated in the same chip. Drawn line width and space are 0.12μm each. R represents a correlation coefficient.

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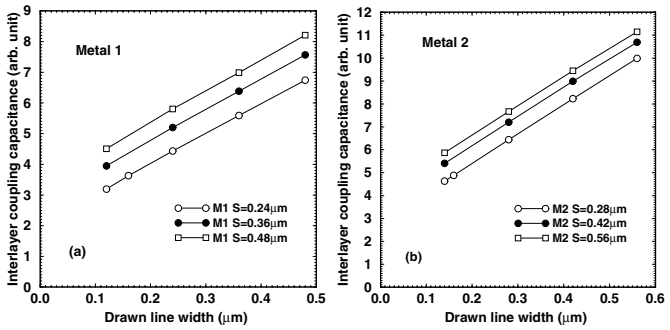

Fig. 6. Drawn line width dependence of interlayer coupling capacitance in the metal 1 and 2 layer with a parameter of drawn line space.

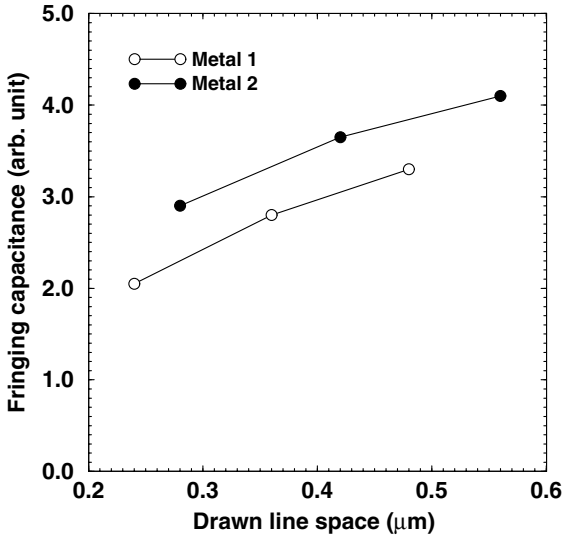

Fig. 7. Drawn line space dependence of fringing capacitance in the metal 1 and 2 layer.

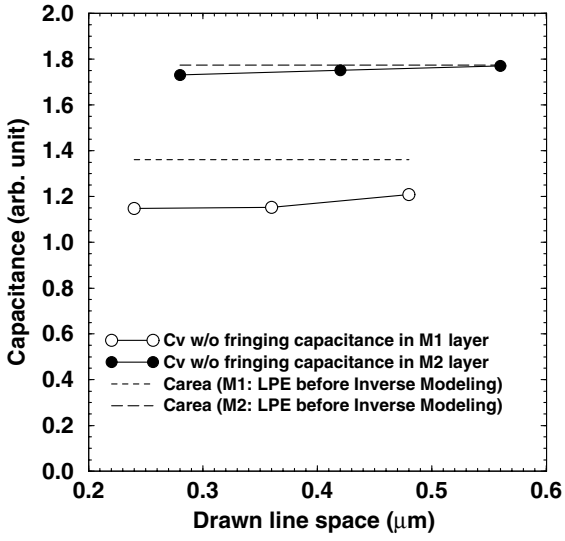

Fig. 8. Drawn line space dependence of interlayer coupling capacitance without fringing capacitance [i.e., $C_{\rm area}$ in (3)] in the metal 1 and 2 layer.

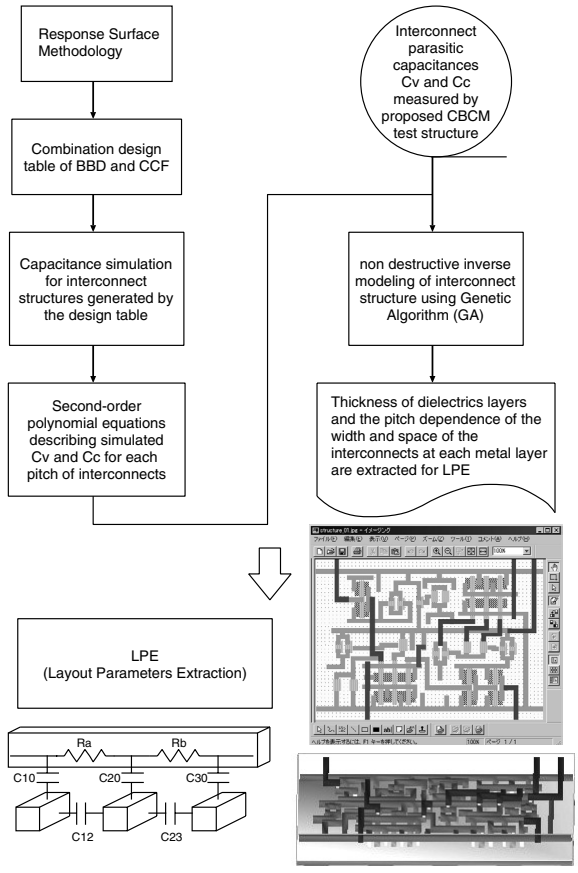

Fig. 9. Flow chart of proposed non-destructive inverse modeling of copper interconnect structures.

the correlation coefficient R of 0.905. Therefore, intralayer coupling capacitance is a sensitive monitor for CD (Critical Dimension) shift of line width.

Fig. 6 shows the measured interlayer coupling capacitance as a function of drawn line width with a parameter of the drawn line space in the metal 1 and 2 layer, respectively. Based on the simple parallel plate model, the interlayer coupling capacitance C_v is composed of the area component C_{area} and the fringing component C_{fringe};

$$C_v = C_{area} \times W \times L + C_{fringe} \times L \qquad (3)$$

where W and L represent wire width and wire length, respectively. Fig. 7 shows the fringing capacitance as a function of drawn line space which is extracted from Fig. 6. The contribution of the fringing capacitance to the interlayer coupling capacitance ranges from 64.1% to 73.2% for the metal 1 layer and from 62.6% to 69.8% for the metal 2 layer. Fig. 8 shows the area component of the measured interlayer capacitance in comparison with that of the simulated one before inverse modeling. The area component has an almost same value regardless of the drawn line space, which confirms the validity of the proposed CBCM test structure. The deviation of the measured capacitances from the simulated ones is primarily due to the ILD thickness variation.

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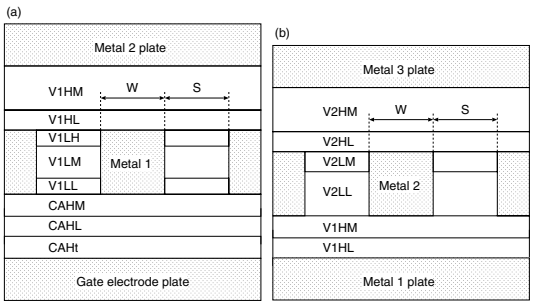

Fig. 10. Cross-sectional view of line and space structure of metal 1 and 2 layer. Rectangular shape is assumed for the cross-sectional shape of interconnect for simplicity.

TABLE I

RATIO OF EXTRACTED THICKNESS TO DESIGNED THICKNESS OF DIELECTRIC LAYERS.

Name of dielectric layer	Ratio of extracted thickness to designed thickness
V2HM	0.860
V2HL	0.942
V2LM	0.994
V2LL	0.951
V1HM	1.124
V1HL	1.073
V1LH	0.989
V1LM	1.177
V1LL	1.116
CAHM	1.144
CAHL	1.161
CAHt	1.122

III. METHODOLOGY OF INVERSE MODELING

Fig. 9 shows a flow chart of non-destructive inverse modeling of copper interconnect cross-sectional structures. The proposed inverse modeling employs the technique of Response Surface Methodology (RSM) [3]. Intra- and interlayer coupling capacitances are described by second-order polynomial equations for each pitch of the interconnects. The thickness of dielectric layers as well as the width and space of interconnects are employed for factors of the equations. The simulated interconnect cross-sectional structures are selected by the combination design table of the Box-Behnken design (BBD) and the Central Composite Factorial (CCF) design [3] for the accurate description. The interconnect cross-sectional structure and the pitch dependence of the interconnect width and space are inversely modeled using the equations in such a way as to reproduce the coupling capacitances measured by the proposed test structures. Genetic Algorithm (GA) is employed for the search engine in the present study. Linear scaling of fitness function in GA was effective to achieve about 100 times speed up of convergence.

Fig. 10 shows the cross-sectional view of the metal 1 and 2 interconnect structure which consists of several dielectric layers, respectively. Rectangular shape is assumed for the cross-sectional shape of copper interconnect for simplicity.

TABLE II

EXTRACTED SPACE AND LPE (AFTER INVERSE MODELING) RELATIVE ERROR TO THE MEASURED CAPACITANCES IN THE METAL 1 LAYER.

drawn line width (μm)	drawn line space (μm)	extracted line space (μm)	relative error of C_c (%)	relative error of C_v (%)
0.12	0.12	0.117	0.033	-0.510
0.12	0.14	0.137	0.040	-0.492
0.12	0.16	0.158	0.023	-0.225
0.12	0.22	0.233	0.074	-0.417
0.12	0.24	0.254	0.066	-0.344
0.12	0.26	0.280	0.121	-0.544
0.12	0.36	0.375	0.040	-0.131
0.12	0.48	0.502	0.217	-0.584
0.14	0.12	0.113	0.029	-0.552
0.14	0.14	0.134	-0.005	0.070
0.16	0.20	0.200	0.043	-0.330
0.16	0.24	0.242	0.059	-0.369
0.24	0.17	0.149	0.009	-0.195
0.24	0.24	0.229	-0.003	0.022
0.24	0.36	0.359	-0.026	0.126
0.24	0.48	0.482	-0.003	0.007
0.36	0.17	0.147	-0.017	0.537
0.36	0.24	0.225	-0.036	0.403
0.36	0.36	0.353	-0.050	0.299
0.36	0.48	0.479	-0.026	0.121
0.48	0.17	0.136	-0.401	0.732
0.48	0.24	0.209	-0.051	1.08
0.48	0.36	0.342	-0.076	0.600
0.48	0.48	0.464	-0.090	0.501

Table I and II show the results of inverse modeling with respect to the metal 1 and 2 layer; Table I shows the ratio of extracted thickness to designed thickness of the dielectric layer while Table II shows extracted line space and LPE (after inverse modeling) relative error to the measured coupling capacitances in the metal 1 layer. Actual pitch of interconnect is assumed to be same as drawn pitch. ILD thickness and line space at each pitch were inversely modeled in such a way as to reproduce the measured coupling capacitances within about 1% error.

IV. CONCLUSIONS

We have presented a new test structure which measures intra- and interlayer coupling capacitance parasitic to copper interconnect, respectively. The test structure not only provides the accurate assessment of actual capacitance variation but provides valuable feedback on the variability of physical parameters such as ILD thickness and interconnect line width. In addition, we have demonstrated methodology to determine the interconnect structures by inverse modeling based on RSM, reproducing the pitch dependence of the measured coupling capacitances. The proposed methodology ensures the accuracy of LPE for 90nm technology node and beyond.

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