CLIMATE (Chip-Level Intertwined Metal and Active Temperature Estimator)

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ULSI interconnect temperature is critical for electromigration risk assessment because of the exponential dependence of lifetime on temperature and for performance issues such as timing which are sensitive to temperature-dependent resistance.

Steady state wire temperature is a function of Joule self-heating within the wire, heat conducted along the wire, and heat coupled from the active devices and other nearby wires through the dielectric. Chip-level estimates of wire temperatures for HP's EV79 microprocessor require rapid processing of vast circuits and thus detailed physical calculations such as those based on 3D finite element models (FEM) are inappropriate. However, temperatures on such large devices can be accurately estimated at the resolution of individual segments of wire as extracted by geometric processing of the layout given each segment's relevant geometry, connectivity to other segments, current I_{rms}, and the thermal conductances G^{lat} between them.

I. Isolated Thermal Network

Processing large layouts and back-annotated schematics for interconnect segment geometry, connectivity, and current I_{rms} has been part of Alpha microprocessor physical verification for at least a decade.[1] A net's interconnect layout is fractured into rectangular segments of width w and length L, connected according to the net's topology. Each segment is represented by a Π model with current sources representing the combined, extracted parasitic capacitance to all segments belonging to other nets (Figure 1(b), but lumped to ground. This net is considered "isolated," however, because no knowledge of actual potentials on other nets is used to model its behaviour. In the Π model, $\Box$ represents the segment electrical conductance, $\Box$ represents the parasitic capacitance, and F_0 and F_L are I_{rms} in and out of the segment.

A. Numerical Solution

Heat flow in a single segment can also be approximated using a Π model by combining heat flow along the segment's length with heat flow through the dielectric to a reference temperature and Joule self-heating (Figure 1(a)), although when the segment is a via the dielectric heat conductance term is neglected (Figure 1(b)). The circuit elements take on the values

$$\Box = L/R^{long};\ \Box = G^{lat}L/2;\ \Box = I_{rms}^2 RL \tag{1}$$

where R and R^{long} are segment electrical and thermal resistances per unit length and G^{lat} is segment thermal conductance per unit length to the substrate (neglected on vias). Steady solid heat conduction, like capacitance, obeys Poisson's equation ($\Box$ is thermal conductivity and $\Box$ is the heat source density):

$$\vec{\Box}\cdot\left(\Box\vec{\Box}T\right) = \Box\Box. \tag{2}$$

Thermal conductance G^{lat} between wire segments and between wire segments and the substrate or active regions can be either estimated or extracted from layout. Conservative estimation formulas are based on the conductance between an isolated segment of known width and thickness, infinite length, and its height above the substrate[2]. Extraction from layout using existing capacitance extraction tools (in our case, HILEX[3]) may be performed after replacing all dielectric constants $\Box$ with appropriate values of $\Box$.

This numerical method has been used to estimate temperature in interconnect networks.[4] However, the solution is piecewise linear, and is thus only accurate when the pieces are "short" enough that the curved temperature trajectory is linear over their lengths.

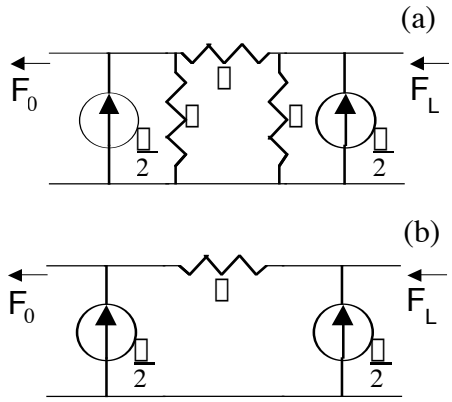

Figure 1 The equivalent circuits used to represent elements of the interconnect network when solving for I_{rms} also solve the system of boundary conditions for segments (a) and vias (b).

B. Analytical Solution

For a temperature calculation valid on segments and vias of arbitrary length, such as those returned for electrical circuit analysis by algorithms which fracture interconnect layout based on corners and changes in width, consider the steady 1D heat equation along a segment (a special form of Poisson's equation),

$$\Box = I_{rms}^2 R = \Box 1/R^{long}\frac{\mathrm{d}^2 T}{\mathrm{d}x^2} + G^{lat}T, \tag{3}$$

where $T(x)$ is the temperature along the segment or via, $T(x=0)=T_0$ and $T(x=L)=T_L$. It has the solutions

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$$T(x)=\frac{\left(T_L-\left(T_0-\right)/G^{lat}\right)\cosh(L)}{\sinh(L)}\sinh(x) \\ +\left(T_0-\right)/G^{lat}\cosh(x)+\left)/G^{lat}, \quad (4)$$

which is valid on segments, where = ($R^{long}G^{lat}$), and

$$T(x)=\left(\frac{R^{long}x^2}{2}+\left(\frac{T_L-T_0}{L}+\frac{R^{long}L}{2}\right)x+T_0, \quad (5)$$

which is valid on vias (G^{lat}=0).

From Eq. (4), the piecewise linear approximation is generally only valid for segments of length $L<1/\sqrt{R^{long}G^{lat}}$, beyond which temperature trajectories may not be linear, as seen in the long trajectories with curved ends in Figure 2.

The analytical formula for temperature may be cast into the form of the model of Figure 1, so that temperature can then be evaluated on a complex net by methods already used for electrical potential.

The thermal flux $F_0=1/R^{long}\mathrm{d}T/\mathrm{d}x$ at x=0 may be computed on a segment:

$$F_0=\frac{-T_0}{R^{long}\tanh(L)}+\frac{T_L}{R^{long}\sinh(L)}+\frac{(\cosh(L)-1)}{\sinh(L)} \quad (6)$$

and on a via

$$F_0=\frac{-T_0}{R^{long}L}+\frac{T_L}{R^{long}L}+\frac{L}{2}. \quad (7)$$

From Kirchoff's Current Law at x=0 (Figure 1(a)),

$$F_0=(+)T_0+T_L+/2. \quad (8)$$

Comparing coefficients with Eq.(6), the element values are

$$=\frac{}{R^{long}\sinh(L)};\quad =\frac{(\cosh(L)-1)}{R^{long}\sinh(L)};\quad \frac{}{2}=\frac{(\cosh(L)-1)}{\sinh(L)}. \quad (9)$$

The element values on a via,

$$=\left(R^{long}L\right)^{-1};\quad =L, \quad (10)$$

are obtained the same way.[5]

The electrical network solution obtained by the software used to develop Alpha microprocessors is only evaluated after it has been obtained symbolically. This facilitates a second evaluation with different numerical values. By substituting the thermal element values from Eqs. (9) and (10) for the electrical element values, it is simple to obtain the temperature solution immediately following the electric current calculation. In fact, this incurs a *negligible* incremental computational burden beyond the existing effort to compute current.

Typical temperature solution trajectories are seen in a 3D visualisation in Figure 2. Even the longest trajectories in the figure correspond to a single segment.

For an infinitely long, isolated wire segment there is a constant solution $T=/G^{lat}$. This solution has formed the basis of previous automated approaches to restricting interconnect self-heating temperature. Its advantages are that on each segment it is easily computed from I_{rms} and independent of other segments. Its disadvantages are that few wires are infinitely long and isolated.

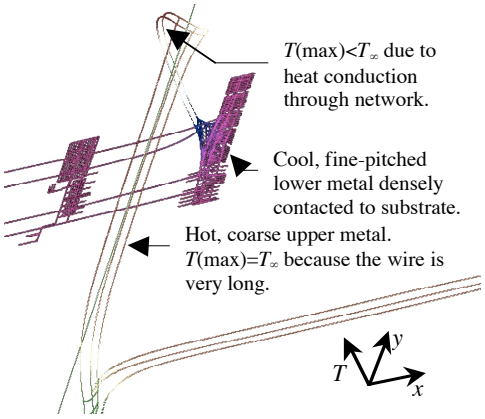

Figure 2 Elevation is temperature $T(x)$ in this visualisation of a VDD fragment from EV7. Each curve is one segment.

Temperature connectivity typically reduces the estimated maximum wire temperatures T(max) of segments with the most significant self-heating, which would otherwise have (over)estimated temperatures T (Figure 3). Since these are the segments which engineers must change in order to meet overall reliability goals, use of T(max) leads directly to savings in unnecessary design activity. Another benefit is that self-heating in vias is also accounted for in T(max), revealing some hot spots unidentifiable by T .

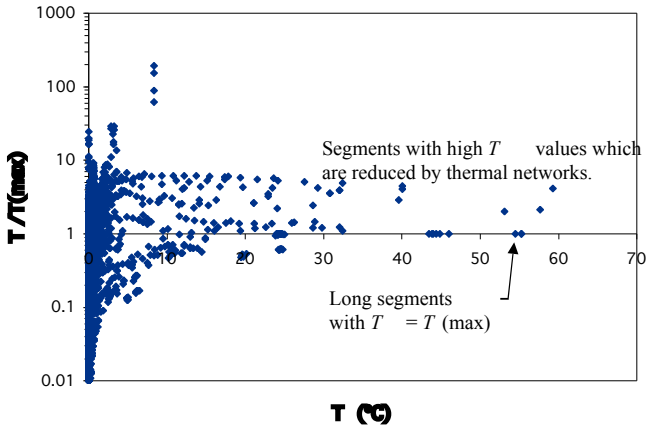

Figure 3 Thermal networks typically reduce the estimated temperature of the hottest segments (i.e. T_∞ /T(max)>1), as seen in this sample from the VDD net in Figure 2 (with 1.06x10^6 segments in the net).

II. Coupled Thermal Network

Since the isolated network solution neglects thermal coupling between nets, it may still be improved upon. Neighbouring nets may couple significant heat to each other, with sets of closely spaced, high-current, parallel wires representing a particularly hot configuration. CLIMATE (Chip-Level Intertwined Metal and Active Temperature Estimator) addresses these dangers, which become greater with increasingly interconnect-dominated chips.

A. Numerical Solution

CLIMATE solves the numerical heat transfer matrix which links the segments in the thermal problem using conductances extracted by HILEX. This matrix is generalised from the isolated network of the previous section by considering conservation of heat at the midpoint of each segment i:

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$$\sum_j \frac{2(T_i - T_j)}{R_i^{long} + R_j^{long}} + \sum_k G_{i,k}^{lat}(T_i - T_k) = \left(I_i^{rms}\right)^2 R_i. \quad (11)$$

In this equation, j and k are indices for segments, which are linked to segment i either through an adjacent metal connection (j) or through the dielectric (k). Also, in this equation R_i^{long}, R_i, and $G_{i,k}^{lat}$ are no longer expressed per unit length but are the total values for these segments.

The large number of segments into which interconnect layout is fractured by conventional algorithms and their topology is unsuitable for CLIMATE. Thus, several automatable, heuristic steps are taken to both reduce the coupled network and place it in the form of Eq. (11): the junctions of multiple segments are converted to pair-wise form using the Y-Δ transform; the resistances of vias attached to only one segment on a layer are merged into the resistances of that segment; and series and parallel segments on the same metal layer are combined into "compound" segments and excessively long segments subdivided to ensure that $L < 1/\sqrt{R^{long} G^{lat}}$ remains valid on each one.

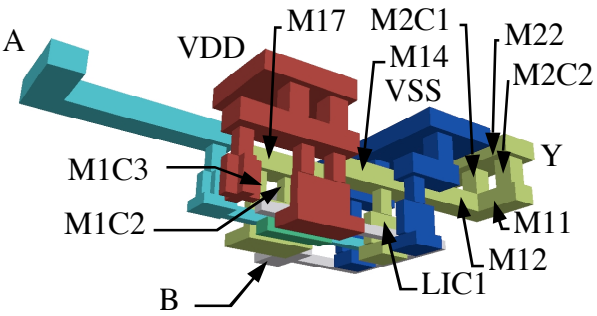

Figure 4 NOR gate interconnect for nets A, B, VDD, VSS, and Y, with some Y-segments and vias indicated.

B. *Example: a Single Gate*

Interconnect temperatures on a NOR gate ($Y = \overline{A + B}$) (Figure 4) are compared between the STAP 3D FEM code[6], the isolated network analytical solution, and CLIMATE. Consider the contrived case where Y bears I_{rms}= 1 A from the remote end of segment Y_M21 to the substrate through Y_LIC2 (Figure 5(a)). The initial fracturing follows geometrical features of the layout, which for net Y results in the topology of Figure 5(a). HILEX extracts the G^{lat} values between each original segment and the substrate and between segments on different nets in less than a second, while STAP (when used as an extraction engine) requires 4.6 hours on a Compaq XP1000 workstation. Simple resistance formulas give each segment's R and R^{long}.

The isolated network analytical solution is evaluated on this topology, using STAP extractions from long, isolated wires as G^{lat} estimates. STAP temperatures are also reported on these segments, but the FEM calculation itself is unaffected by segmentation.

For CLIMATE, the NOR gate interconnect is restructured into 23 compound segments (Figure 5 shows the process for net Y, Figure 6 locates the compound segments). A 23x23 heat transfer matrix between the midpoints of these compound segments is constructed using Eq. (11). All compound segments satisfy the thermal length criterion (Figure 7).

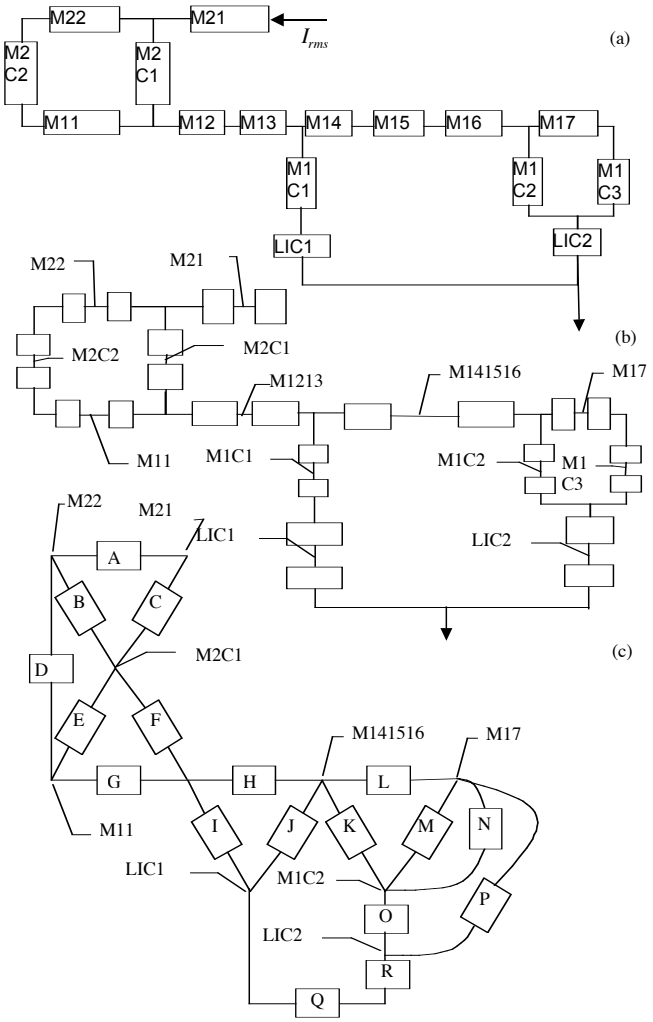

Figure 5 (a) The initial Y-net topology prior to formation of compound segments. (b) Assignment of segment properties to segment ends. (c) Formation of Eq. (11) matrix elements, labeled A-R Electric current flows only through the LIC2 contact to ground, but heat flows also through LIC1.

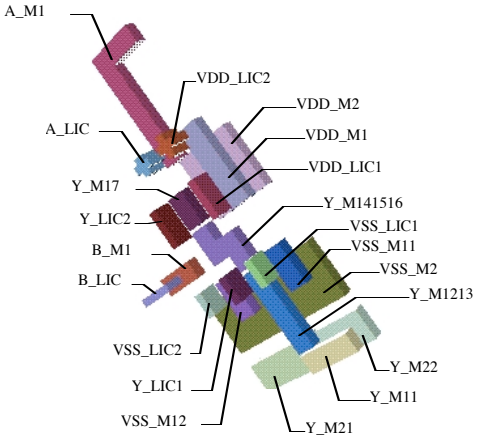

Figure 6 Compound segmentation of the NOR gate (21 of 23 shown), seen from below. The segment Y_M21 origin is at the very bottom of the figure.

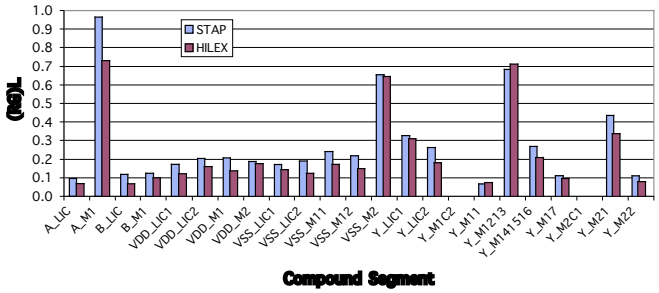

Figure 7 The one-dimensional thermal length criterion, $(R^{long}G^{lat})L<1$, is satisfied on each compound segment of the NOR cell's interconnect. The HILEX extraction of G^{lat} is challenged by this highly 3-dimensional layout, but its accuracy is acceptable (STAP-extracted G^{lat} is presumably correct).

The temperature trajectory along Y (Figure 8) descends from the origin of segment Y_M21 (BC: ∂T=0) to the substrate (BC: T=0), including the loops.[7] The analytical solution conservatively overestimates temperature relative to STAP, largely by neglect of thermal conductance to the substrate from vias and the exposed segment ends. However, STAP slightly underestimates via temperature drops since its as-drawn, square vias have too much surface area and thus higher thermal conductance than the circular vias which are actually formed on the chip. Inclusion of the passive nets (A, B, VDD, and VSS) reduced the STAP-estimated temperatures on Y. CLIMATE temperatures on each segment of Y closely matched STAP's averages (when all nets were included).

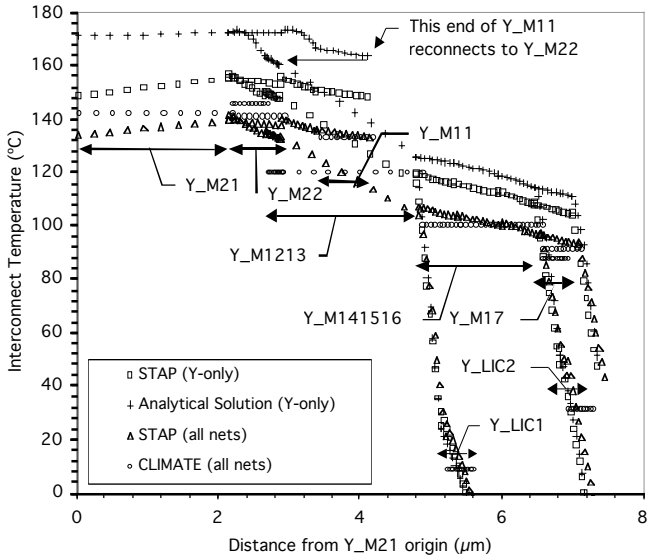

Figure 8 Self-heating temperature along the Y-net in isolation and coupled to passive nets calculated by different methods.

Figure 9 compares CLIMATE temperatures with STAP averages on all segments. Agreement on passive nets was adequate for large, strongly coupled segments, but there is clearly scope for refinement. The differences are due both to the inaccuracies of HILEX's G^{lat} extraction and the approximation inherent in the numerical network. For example, HILEX extracts G^{lat}=0 between segments with very minor coupling. The potential accuracy of the numerical solution is seen in the temperatures recalculated using highly accurate, STAP-extracted G^{lat} values. For some segments agreement is improved and for others it is worsened, with deviations from the STAP temperatures similar to CLIMATE's. The two sources of error (G^{lat} extraction and piecewise linearity of the numerical solution) are thus of comparable size for this case.

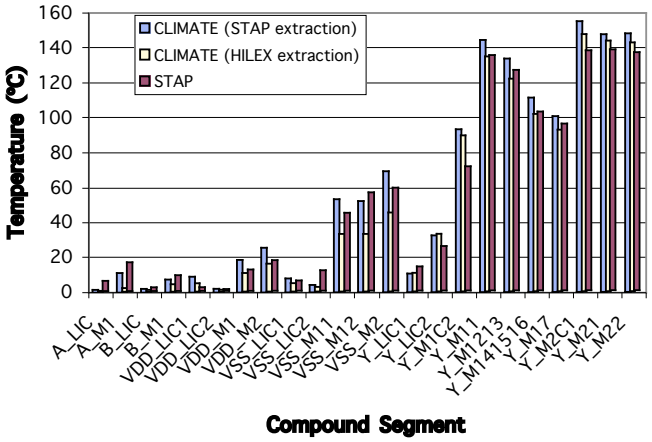

Figure 9 Comparison of CLIMATE temperatures based on both HILEX and STAP G^{lat} extractions and temperatures from STAP shows CLIMATE's accuracy is affected by both the G^{lat} extraction and the numerical solution on compound segments.

This CLIMATE example shows the feasibility of rapid, automated, coupled, interconnect temperature estimation on regions much larger than those soluble by field solvers. A full chip may be decomposed into as many such regions as necessary, to be solved in parallel. Wafer and package thermal transport, based on transistor power dissipation, is already routinely computed and can either define a regional substrate temperature boundary condition or CLIMATE-solved regions can be integrated directly into chip-scale models. CLIMATE should enable high-resolution interconnect temperature estimation for the largest of ULSI devices.

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[2] D. Harmon, J. Gill, and T. Sullivan, "Thermal Conductance of IC Interconnects Embedded in Dielectrics," Integrated Reliability Workshop Final Report, 1-9, 1998.

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[4] Chin-Chi Teng, Yi-Kan Cheng, Elyse Rosenbaum, and Sun-Mo Kang, "iTEM: A Chip-Level Electromigration Reliability Diagnosis Tool Using Electrothermal Timing Simulation," International Reliability Physics Symposium, 172-179, 1996.

[5] Andrew Labun and James Jensen, "One-Dimensional Estimation of Interconnect Temperatures," International Integrated Reliability Workshop Final Report, 157-161, 2002.

[6] Rainer Sabelka, Kazuhide Koyama, and Siegfried Selberherr, "STAP - A finite element simulator for three-dimensional thermal analysis of interconnect structures," Proc. Simulation in Industry - 9th European Simulation Symposium, 621-625, 1997.

[7] STAP reports minimum and maximum temperatures on each segment but not trajectories. The graph shows linear interpolations between these extrema, which are assigned to opposite ends of their respective segments.

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