Experimental Study on Carrier Transport Mechanism in Ultrathin-body SOI MOSFETs

Ken Uchida*, Hiroshi Watanabe, Junji Koga, Atsuhiro Kinoshita, and Shin-ichi Takagi
Advanced LSI Technology Laboratory, Toshiba Corp., 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
*E-mail: k-uchida@amc.toshiba.co.jp

***Abstract*— The electrical characteristics of ultrathin-body SOI CMOSFETs are intensively investigated. It is demonstrated that electron mobility increases as SOI thickness decreases, when SOI thickness, T_{SOI}, is in the range from 3.5 nm to 4.5 nm. On the other hand, hole mobility decreases monotonically as T_{SOI} decreases. In addition, it is demonstrated that, when SOI thickness is thinner than 4 nm, slight (even atomic-level) SOI thickness fluctuations have a significant impact on threshold voltage, gate-channel capacitance, and carrier mobility of ultrathin-body CMOSFETs.**

Keywords- ultrathin-body, SOI, MOSFET, mobility, quantum-mechanical confinement

I. INTRODUCTION

Ultrathin body (UTB) SOI MOSFETs are promising candidates for a sub-30-nm MOSFET structure. In order to utilize the UTB MOSFETs in the deep-sub-20-nm regime, the realization of sub-5-nm SOI films is essential. Although much theoretical work has been done on the electrical characteristics of UTB MOSFETs [1-4], there are only a few experimental works [5-13]. Therefore, the electrical characteristics of UTB MOSFETs have not been fully understood yet.

In this report, the electrical characteristics of UTB CMOSFETs with SOI thickness, T_{SOI}, ranging from 2.3 nm to 13 nm are intensively investigated. As a result, it is shown that electron mobility of UTB MOSFETs with T_{SOI} of greater than 6 nm shows no T_{SOI} dependence at low temperatures [14], indicating that the room-temperature mobility degradation in UTB MOSFETs with T_{SOI} of less than 20 nm is mainly due to the phonon scattering. It is demonstrated for the first time that electron mobility increases as T_{SOI} decreases, when T_{SOI} is in the range from 3.5 nm to 4.5 nm [15]. It is also demonstrated that, when T_{SOI} is thinner than 4 nm, slight (even atomic-level) SOI thickness fluctuations have a significant impact on threshold voltage, gate-channel capacitance, and carrier mobility of UTB CMOSFETs [15]. In addition, the relevance of a new type of scattering mechanism, that is, SOI-thickness-fluctuation- induced scattering is pointed out and experimentally verified [15].

II. DEVICE STRUCTURE

Ultrathin-body (UTB) CMOSFETs with thick source and drain regions were fabricated using UNIBOND wafers with 10Ωcm p-type 200-nm Si film over 400-nm buried oxide (Fig. 1). Fig. 2 shows a TEM image of a fabricated SOI channel, indicating the successful fabrication of ultrathin, 2.4-nm-thick SOI channel. The SOI channels were left undoped for both n- and p-MOSFETs.

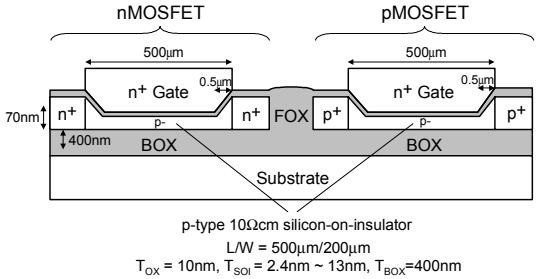

Fig.1. Schematic of fabricated SOI CMOSFETs. The channel of both n- and p-MOSFETs is p-type 10Ωcm SOI, and its thickness is varied from 2.3 nm to 13 nm.

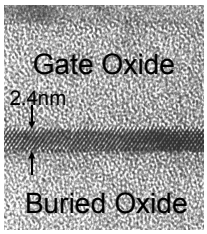

Fig.2. TEM image of fabricated SOI channel. Successful fabrication of ultrathin (2.4nm) SOI channel is confirmed.

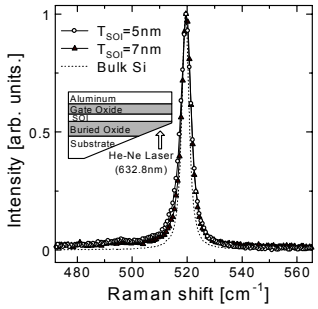

Fig. 3: Raman spectra of ultrathin SOI films. Raman spectrum of bulk Si is also indicated as a reference. The spectrum of the ultrathin SOI films is similar to that of bulk Si, showing that there is no significant residual stress in ultrathin SOI films.

Since residual stress in the channel of MOSFETs strongly affects carrier mobility, residual stress in the ultrathin SOI channel should be evaluated. Raman spectra of ultrathin (5-nm and 7-nm) SOI layers were taken, utilizing slanting-polish-from-backside and laser-illumination-through-buried-oxide techniques. The schematic of the prepared sample is shown in the inset of Fig. 3. As shown in Fig, 3, the Raman spectra of ultrathin SOI films are almost the same as the Raman spectrum of bulk Si, indicating that there is no significant residual stress in the ultrathin SOI films.

III. T_{SOI} DETERMINATION

In order to investigate the T_{SOI} dependence of UTB CMOSFET characteristics, it is essential to precisely determine the thickness of SOI channel. Therefore, the relative comparison of SOI thickness is firstly performed using the substrate-bias-induced V_{th} shifts. Since the effect of substrate bias on the V_{th} shift is less in thinner body CMOSFETs, smaller V_{th} shift corresponds to thinner T_{SOI}. Fig. 4 depicts the measured relationship between V_{th}'s and V_{th} shifts in UTB CMOSFETs. The V_{th} increase in thinner T_{SOI} in both n- and p-MOSFETs suggests that the subband energy level increase is due to quantum-mechanical confinement effects in ultrathin SOI channel. The universal relationship between V_{th}'s and V_{th} shifts confirms that the variation of UTB CMOSFET characteristics is dominated by T_{SOI} variation and that the variations of other device parameters, such as gate-oxide thickness, buried-oxide thickness, and substrate impurity concentration, are sufficiently suppressed and have negligible effects on UTB CMOSFET characteristics.

Next, in order to determine the actual SOI thickness, several TEM images are obtained, and the relationship between the T_{SOI}'s and V_{th} shifts is empirically determined (Fig. 5). As a result, T_{SOI}'s are now precisely estimated from the substrate-bias-induced V_{th} shift.

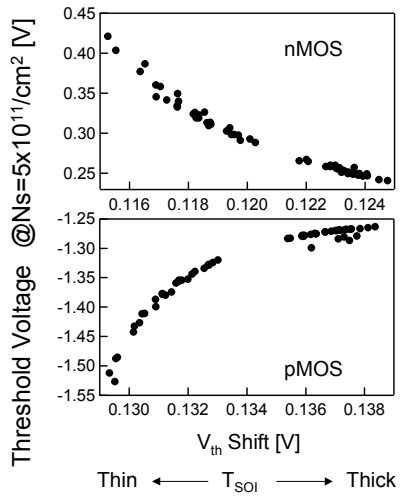

Fig.4. Threshold voltage shift versus threshold voltage of UTB CMOSFETs.

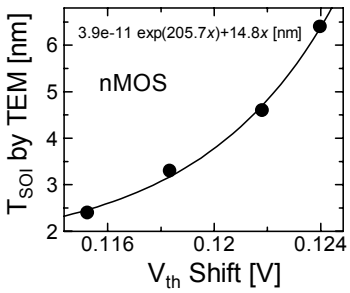

Fig.5. Threshold voltage shift versus SOI thickness measured by TEM.

IV. MOBILITY CHARACTERISTICS

First, the electrical characteristics of UTB nMOSFETs with T_{SOI} of greater than 8 nm are investigated. Fig. 6 shows effective electron mobility μ_{eff} versus effective field, E_{eff}, characteristics of UTB MOSFETs at room temperature. The mobility of a 68-nm SOI MOSFET almost coincides with the bulk universal mobility. This SOI MOS-FET is therefore referred to as a bulk-like SOI MOSFET in the following part of this article. The decrease of μ_{eff} with a decrease in T_{SOI} is observed, which quantitatively agrees with the previously reported results [3,4].

In order to investigate the physical origin of μ_{eff} degradation, the μ_{eff}-E_{eff} characteristics were measured over wide temperature ranges in relatively thicker UTB SOI MOSFETs, whose SOI channel thickness in the range from 7 nm to 13 nm. As shown in Fig. 7, the difference of the mobility between the UTB MOSFETs and the bulk-like SOI-MOSFET becomes large in low E_{eff} regions as temperature decreases. However, at temperatures lower than 100K, the electron mobility of 8.7-nm and 12.4-nm UTB MOSFETs, whose mobility is lower than bulk-MOSFET mobility at room temperature, coincides with that of thick, bulk-like SOI-MOSFET, as shown in Fig. 8. This result indicates that, in UTB MOSFETs with T_{SOI} of greater than 8 nm, 1) SOI

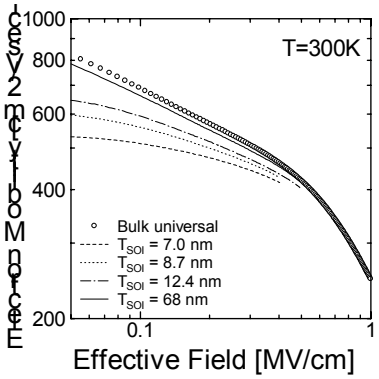

Fig. 6. Effective electron mobility versus transverse effective field of ultrathin body (UTB) SOI MOSFETs for various SOI thickness. The electron mobility of UTB MOSFETs decreases with a decrease in the SOI thickness.

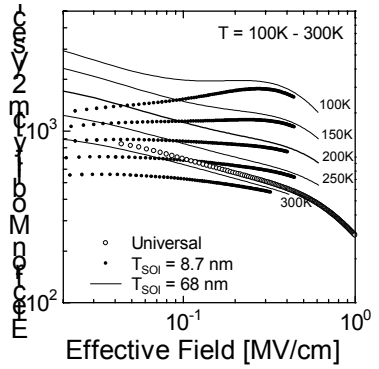

Fig. 7. Effective electron mobility of ultrathin (T_{SOI}=8.7nm) and thick (T_{SOI}=68nm) SOI MOSFETs as a function of transverse effective field for various temperatures (100K ~ 300K). The mobility of the 8.7-nm UTB MOSFETs is less than that of the 68-nm, bulk-like SOI MOSFET.

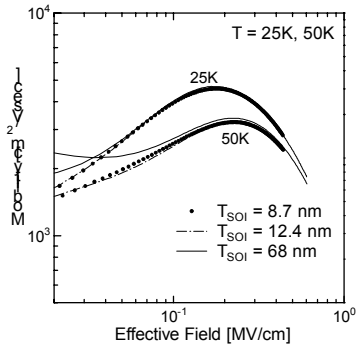

Fig. 8. Effective electron mobility of 8.7-nm, 12.4-nm, and 68-nm SOI MOSFETs as a function of transverse effective field at the temperatures of 25K and 50K. The mobility of the 8.7-nm and 12.4-nm SOI MOSFETs coincides with that of the 68-nm, bulk-like SOI MOSFET.

thickness of UTB MOSFETs is so uniform that there is no scattering center resulting from thickness fluctuations and that 2) the effect of Coulomb scattering and roughness scattering on the electron mobility in UTB MOSFETs with T_{SOI} of greater than 8 nm is basically the same as that in bulk MOSFETs, at least at low temperatures. These results indicate that room-temperature mobility degradation in UTB MOSFETs is mainly caused by phonon scattering.

Next, the characteristics of UTB CMOSFETs with T_{SOI} of less than 8 nm are investigated. Fig. 9 shows the hole mobility, μ_h, versus effective field, E_{eff}, characteristics for various T_{SOI}'s. In the whole E_{eff} regions, hole mobility decreases as T_{SOI} decreases. Although the increase of hole mobility in T_{SOI} thinner than 5 nm was previously reported, no theoretical explanation for the hole mobility enhancement in thinner T_{SOI}

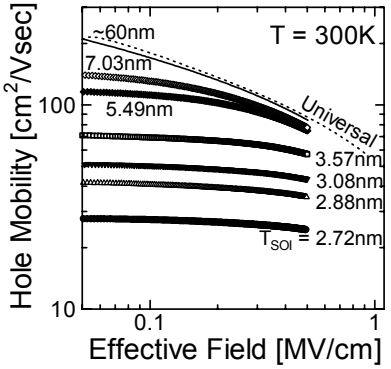

Fig.9. Hole mobility versus effective filed for various T_{SOI}'s at 300 K.

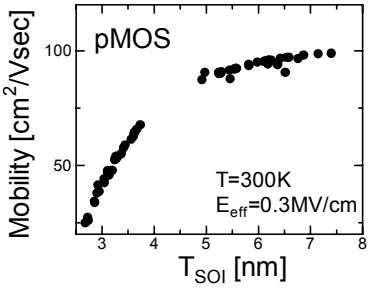

Fig.10. T_{SOI} dependence of hole mobility at 300 K. The hole mobility decreases monotonically as T_{SOI} decreases.

has been made. Our results (Fig. 10) show the clear monotonic decrease of μ_h with a decrease of T_{SOI}. The decrease of hole mobility in thinner T_{SOI} can be attributed to the increase of phonon scattering, because phonon scattering increases as T_{SOI} decreases.

Fig. 11 shows the electron mobility, μ_e, verses E_{eff} characteristics for various T_{SOI}'s. Although, at E_{eff} lower than 0.1MV/cm, electron mobility decreases with a decrease of T_{SOI}, an enhancement of electron mobility with a decrease of T_{SOI} is observed at E_{eff} of around 0.3 MV/cm. Fig. 12 shows the T_{SOI} dependence of μ_e at the E_{eff} of 0.3 MV/cm. It should be noted that, when T_{SOI} is in a range from 3.5 nm to 4.5 nm, electron mobility increases as T_{SOI} decreases. The increase of μ_e with a decrease of T_{SOI} in T_{SOI} ranging from 3 nm to 5 nm has been theoretically predicted [3,4]. The good agreement of SOI thickness range, where mobility increase is observable, between the present experimental work and theoretical work [3,4] suggests that the enhancement is due to subband level modulation by quantum-mechanical confinement effects in ultrathin SOI film, as suggested in the theoretical work, though the observed mobility enhancement is smaller than theoretically predicted enhancement.

V. Effect of δT_{SOI} on C-V and I-V characteristics

In order to clarify the reason for the smaller electron mobility enhancement than the predicted one, C-V and I-V

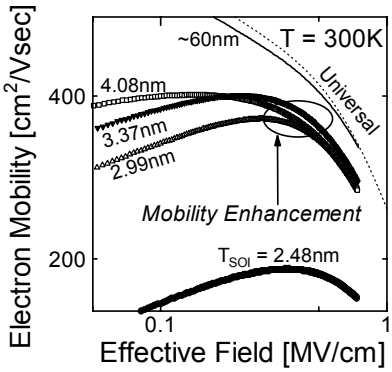

Fig.11. Electron mobility versus effective field for various T_{SOI}'s at 300 K. Electron mobility increase in thinner T_{SOI} is observed at E_{eff} of around 0.3 MV/cm.

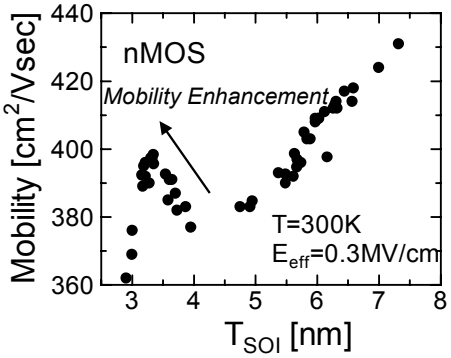

Fig.12. T_{SOI} dependence of electron mobility at 300 K. Electron mobility increases as T_{SOI} decreases, when T_{SOI} is in a range from 3.5nm to 4.5 nm.

characteristics of UTB CMOSFETs are thoroughly compared with self-consistent calculation results of Schrödinger and Poisson equations. In order to examine the influence of T_{SOI} on C_{gc} with higher sensitivity, the derivative of C_{gc} with respect to V_g, that is, dC_{gc}/dV_g, is utilized. Fig. 13 shows T_{SOI} dependence of dC_{gc}/dV_g. As shown in the figure, the increase of theoretical dC_{gc}/dV_g with a decrease of T_{SOI} is clearly observed, which is due to the quantum-mechanical confinement effects of carriers in ultrathin SOI. However, when T_{SOI} is thinner than 4 nm, experimental dC_{gc}/dV_g decreases with a decrease of T_{SOI}.

Fig. 14 shows the T_{SOI} dependence of V_{th}'s of UTB nMOSFETs. Although the experimental V_{th}'s agree well with theoretical ones when T_{SOI} is greater than 4 nm, additional V_{th} increase is observed in T_{SOI} of less than 4 nm. Fig. 15 shows V_{th}'s of UTB pMOSFETs as a function of T_{SOI}. Additional V_{th} increase compared to the theoretical one is also observed.

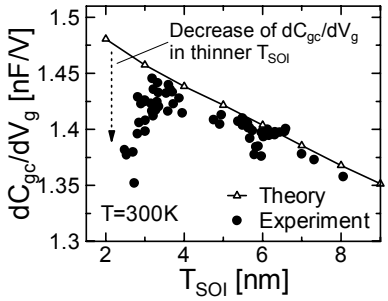

Fig.13. SOI thickness dependence of dC_{gc}/dV_g at C_{gc} of 150pF. Experimental and theoretical (self-consistent calculation) results are shown. Deviation from theoretical curve (degradation of dC_{gc}/dV_g) is clearly observed in T_{SOI} thinner than approximately 4 nm.

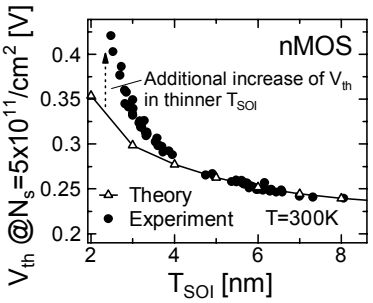

Fig.14. T_{SOI} dependence of nMOS V_{th}. Additional V_{th} increase is observed in T_{SOI} thinner than 4nm.

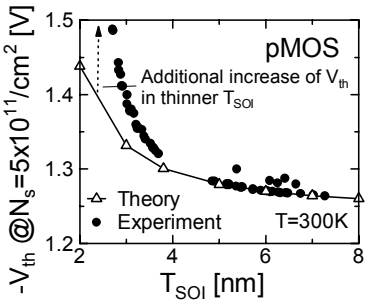

Fig. 15. T_{SOI} dependence of pMOS V_{th}. Additional V_{th} increase is observed as in the case of nMOSFETs.

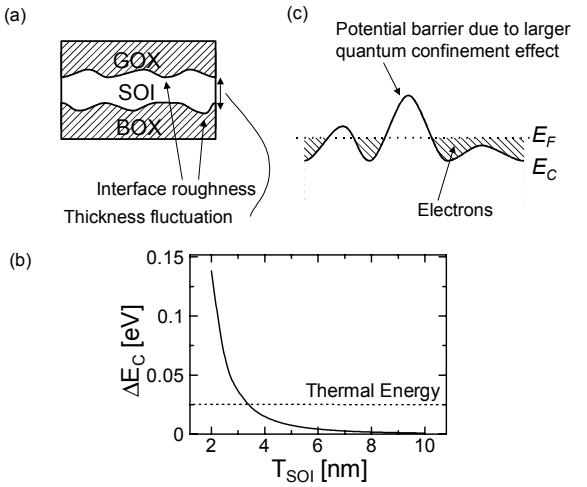

Fig.16. (a) Si/SiO_2 interface roughness induces SOI thickness fluctuations. (b) Variation of conduction band energy level due to SOI thickness fluctuation. The interface roughness of ±1atomic-layer per Si/SiO_2 interface is assumed. (c) Schematics of E_C variation effects.

The degradation of dC_{gc}/dV_g and the additional V_{th} increase in thinner T_{SOI} can be understood in terms of SOI thickness fluctuation, δT_{SOI}. Since Si/SiO_2 interface has ±1 atomic layer interface roughness, it is reasonable to assume that SOI has δT_{SOI} of approximately 4 atomic layers (Fig. 16a). Fig. 16b shows changes in conduction band energy, ΔE_C, induced by 4-atomic-layer δT_{SOI}, as a function of average T_{SOI}. When T_{SOI} is thinner than 4 nm, ΔE_C exceeds the thermal energy at room temperature, meaning that potential barriers due to difference of quantum-mechanical confinement effects from one part to another are formed in the ultrathin SOI channel (Fig. 16c). Therefore, in the case of UTB CMOSFETS having SOI fluctuations, higher gate voltage is necessary to obtain the same surface carrier concentration than in the case of UTB MOSFETs having no SOI fluctuation. As a result, V_{th} increase and slow C_{gc} rise are observed in UTB MOSFETs with SOI thickness fluctuations.

VI. Effect of δT_{SOI} on Mobility Characteristics

Next, the effect of SOI-thickness fluctuations on carrier mobility is discussed. Since the potential barriers shown in Fig. 16b are expected to work as scattering potential for carriers, μ_e and μ_h are expected to decrease as T_{SOI} decreases. In fact, in GaAs/AlAs quantum wells, scattering by GaAs-width-fluctuation-induced potential is reported [16]. It is also reported that the width-fluctuation-limited mobility shows d^6 dependence, where d is the GaAs channel width [16,17].

In order to examine whether this type of scattering is associated or not, μ_e for various T_{SOI}'s is measured at low temperatures, because at low temperature phonon scattering is suppressed and the effect of thickness-fluctuation-induced scattering is observable more clearly. Fig. 17 shows μ_e-E_{eff} characteristics at 25 K, showing monotonic decrease of μ_e with a decrease of T_{SOI}. Fig. 18 shows the T_{SOI} dependence of μ_e at 25 K. The T_{SOI}^6 dependence is clearly observed, meaning that

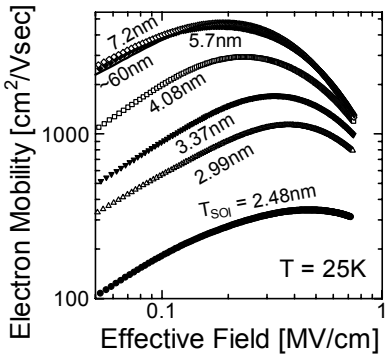

Fig.17. Electron mobility versus effective field at 25K. Electron mobility decreases in the whole E_{eff} regions when T_{SOI} is thinner than approximately 4nm.

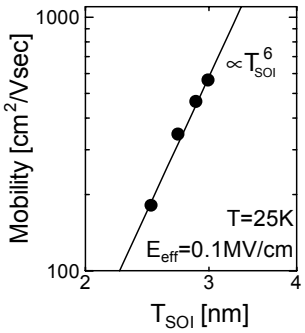

Fig.18. T_{SOI} dependence of electron mobility at 25 K. T_{SOI}^6 dependence indicates that the dominant scattering mechanism is T_{SOI}-fluctuation- induced scattering.

in extremely thin SOI film the μ_e is dominated by scattering due to δT_{SOI}-induced potential. Fig. 19 shows the temperature dependence of μ_e in nMOSFETs with T_{SOI} of 2.48 nm. The temperature dependence is qualitatively the same as that of well-width-fluctuation-limited mobility in quantum wells [16]. Thus, it is concluded that this is the first observation of the relevance of a new type of scattering mechanism, namely δT_{SOI}-induced scattering, peculiar to UTB MOSFETs. Fig. 20 shows the μ_h-E_{eff} characteristics at 25 K. The rapid decrease of μ_h in thinner T_{SOI} suggests that δT_{SOI}-induced scattering is also influential to pMOSFETs. Fig. 21 shows the μ_e-E_{eff} characteristics, where δT_{SOI}-fluctuation-induced scattering is subtracted using Mathiessen's rule. The increase of μ_e with a decrease of T_{SOI} is clearly observed in the whole E_{eff} region, when T_{SOI} changes from 4.08 nm to 3.37 nm. Therefore, it is concluded that the realization of atomically flat SOI is vital (Fig. 22), in order to enjoy the full advantages of UTB CMOSFETs in deep-sub-20-nm regime.

VII. Conclusion

The carrier transport mechanism in UTB CMOSFETs with T_{SOI} ranging from 2.3 nm to 13 nm is investigated. It is demonstrated, for the first time, that electron mobility increases as T_{SOI} decreases, when T_{SOI} is in the range from 3.5 nm to 4.5 nm, because of subband-energy modulation effects. It is also demonstrated that, when T_{SOI} is extremely thin (<4nm), slight (even atomic-level) T_{SOI} fluctuations have a significant impact on V_{th} and C_{gc} of UTB CMOSFETs. In addition, δT_{SOI}-induced

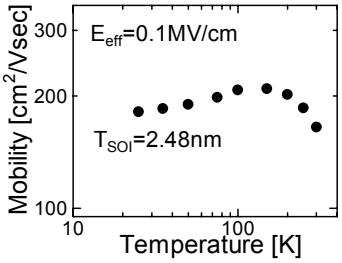

Fig.19. Temperature dependence of electron mobility of 2.4-nm-thick SOI nMOSFET at E_{eff} of 0.1 MV/cm. The temperature dependence is qualitatively the same as that of the well-width-fluctuation-limited mobility in GaAs/AlAs quantum-wells [5].

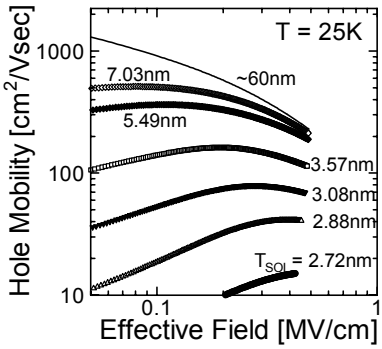

Fig.20. Hole mobility versus effective field at 25 K.

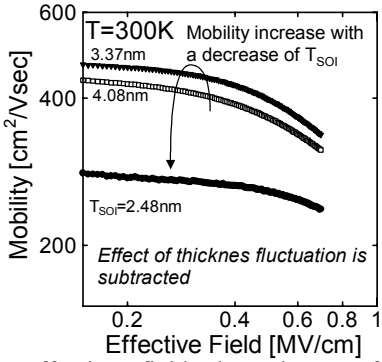

Fig.21. Effective field dependence of electron mobility, where the effect of thickness fluctuation is subtracted.

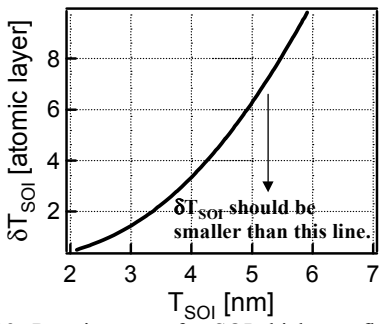

Fig. 22. Requirements for SOI thickness fluctuation, δT_{SOI}, as a function of T_{SOI}, calculated on the assumption that ΔE_C should be smaller than the half of thermal energy at room temperature. 1-atomic layer corresponds to approximately 0.28nm

scattering, which is a new scattering mechanism to strongly limit the mobility of UTB MOSFETs with T_{SOI} of less than 3nm, is observed, for the first time. It should be noted that this type of scattering also limits the mobility of other thin-channel MOSFETs, such as FinFETs [18]. It is concluded that the realization of atomically flat SOI is vital, in order to enjoy the full advantages of UTB CMOSFETs, such as electron mobility enhancement and larger C_{gc} rise, in deep-sub-20-nm regime.

ACKNOWLEDGEMENT

This work was performed under the management of JEITA, which is supported by NEDO.

REFERENCES

[1] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, Tech. Dig. Int. Electron Devices Meet. (2002), p.719.

[2] F. Gámiz, J. B. Roldán, J. A. López-Villanueva, P. Catrujo-Cassinello, and J. E. Carceller, J. Appl. Phys., **86**, 6854, 1999.

[3] M. Shoji and S. Horiguchi, J. Appl. Phys., **85**, 2722, 1999.

[4] S. Takagi, J. Koga, and A. Toriumi, Tech. Dig. Int. Electron Devices Meet. (1997), p.219.

[5] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, IEEE Electron Device Lett., **14**, 569, 1993.

[6] J. Wang, N. Kistler, J. Woo, and C. R. Viswanathan, IEEE Electron Device Lett., **15**, 117, 1994.

[7] J.-H. Choi, Y.-J. Park, and H.-S. Min, IEEE Electron Device Lett., **16**, 527, 1995.

[8] A. Toriumi, J. Koga, H. Satake, and A. Ohata, Tech. Dig. of Int. Electron Devices Meet. (1995), p.847.

[9] D. Esseni, M. Mastrapasqua, G. K. Celler, F. H. Baumann, C. Fiegna, L. Selmi, and E. Sangiorgi, Tech. Dig. Int. Electron Devices Meet. (2000), p.671.

[10] D. Esseni, Tech. Dig. Int. Electron Devices Meet. (2001), p.445.

[11] J. Koga, S. Takagi, and A. Toriumi, IEEE Trans. Electron Devices, **49**, 1042, 2002.

[12] Z. Ren, P. Solomon, T. Kanarsky, B. Doris, O. Dokumaci, P. Oldiges, R. Roy, E. Jones, M. Ieong, R. Miller, W. Haensch, H. Whong, Tech. Dig. Int. Electron Devices Meet. (2002), p.51.

[13] T. Ernst, D. Munteanu, S. Cristoloveanu, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, Microelectronic Eng., **48**, 339, 1999.

[14] K. Uchida, J. Koga, R. Ohba, T. Numata, and S. Takagi, Tech. Dig. of Int. Electron Devices Meet. (2001), p.633.

[15] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, Tech. Dig. of Int. Electron Devices Meet. (2002), p.47.

[16] H. Sakaki, T. Noda, K. Hirakawa, M. Tanaka, and T. Matsusue, Appl. Phys. Lett., **51**, 1934, 1987.

[17] A. Gold, Phys. Rev. B, **35**, 723, 1987.

[18] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, R. Anderson, T.-J. King, J. Bokor, and C. Hu, IEEE Trans. Electron Devices, **47**, 2320, 2000.

