Modeling and Characterization of Copper Interconnects for SoC Design

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ABSTRACT

Interconnect (wiring) is central to nanometer system-on-a-chip (SoC) design. As such, accurate interconnect modeling and characterization are key to the design and verification of SoCs. Today copper (Cu) has become a mainstream material for on-chip interconnections. Unlike aluminum (Al) interconnects, Cu wire line width and thickness is a function of wire width and spacing, wire-pattern density, and topography. These new effects must be modeled accurately for designs to achieve first- time silicon success. In this paper we discusses the Cu process and its impact on modeling the interconnect parasitic elements - resistance (R), capacitance (C), and inductance (L). For a given process node, use of Cu reduces interconnect delay and power, but from a design prospective, the same effect is achieved by reducing wire length. Impact of the X- Architecture, which makes pervasive use of diagonal lines and has the promise of reducing wire length to an average of 20%, is also discussed. Finally, silicon validation of interconnect R,C, and L model using a test-chip approach is covered.

I. INTRODUCTION

Advances in integrated circuit (IC) design and manufacturing are yielding faster and denser circuits with ever-increasing functionalities. The continued down-scaling of the devices and high level of integration of functional blocks (digital, analog, and mixed-signal circuits on the same chip), into the so-called system-on-a-chip (SoC), have traditionally driven down the cost of these chips, but the complexity of design and manufacturing has increased consequently. As time-to-market and time-to-volume becomes very critical, the use of silicon-validated SoC design and verification tools during the design phase becomes more important.

Though the down-scaling of devices has resulted in improved device performance and hence shorter transistor delays (CV/I), the associated interconnect delays (RC) limits this performance [1]. In fact, performance of today's state-of-the art IC is dominated by the performance of interconnects (wires). Since meeting the design challenges of SoC, such as timing closure, signal integrity, power distribution etc., all depend on accurate modeling of interconnect parasitic elements (resistance R, capacitance C and inductance L), a better understanding of interconnects is essential for the design to be first-time functional.

As the scaling continues, process variation grows rapidly, resulting in substantial interconnect process parameter variation. Optical proximity correction (OPC), though necessary for proper processing of the lines, also causes the deviation of the line width from the drawn width. These variations result in variation of the signal delay and cross-talk noise. New processes such as Cu dual damascene and chemical mechanical polishing (CMP) further complicate the design [2]. The worst-case simulation is no longer adequate, and the traditional practice of using excessive performance guard band affects product margin, even profit. *Silicon-accurate interconnect modeling is thus key to the design and verification of nanometer SoCs* [3-4].

II. X-ARCHITECTURE

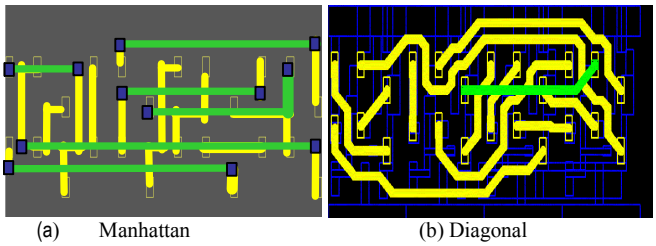
Aluminum (Al) has been de-facto industry standard as a material for interconnects in VLSI chips for over 30 years. However, recently Al has been replaced by Cu in order to reduce both wire resistance and capacitance. In fact the major change in moving from the 180nm technology node to 130nm technology node is the use of Cu as interconnect lines and the use of low-k dielectrics.

The use of Cu and low k material has delayed the transition point, from 250nm process node to 130nm node, where interconnect delay exceeds the transistor delay. Still the interconnect delay is projected to increase significantly as the scaling continues. This is evident from the Table 1 that gives a summary of various delays at different technology nodes based on process data from SIA roadmap 1999 [5]. Clearly, delay decreases going from Al process (180nm node) to Cu process (130nm node), but then going forward it increases again.

Table 1: RC delay for various process nodes.

Process Node	X-section Area	R/µm Ω	C/µm fF	SoC Freq. MHz	jωL/µm	RC Delay/µm
180nm	0.15	0.25	0.15	500	0.01j	0.040
130nm	0.07	0.30	0.12	1000	0.023j	0.036
90nm	0.05	0.40	0.14	1500	0.040j	0.056

Since wire length is a prime factor in circuit delay and chip power consumption, any approach that helps to reduce the wire length will have the same impact as reducing wire RC, thus prompting some fundamental design changes. Recently an "X-Architecture" that makes pervasive use of diagonal



(a) Manhattan (b) Diagonal

Fig. 1 An example of (a) Manhattan layout, (b) and an X-Architecture layout which results in overall shorter wire length.lines (45°) has been

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proposed to replace traditional Manhattan-only routing (see Fig. 1), resulting in reduced interconnect delays for the same technology node.

It has been demonstrated [6] that a chip using the X Architecture has 20+% less interconnect and 30+% fewer vias, resulting in simultaneous improvements in a chip performance, power, and cost.

COPPER INTERCONNECTS

In spite of its advantages, the use of Cu interconnects has its own manufacturing issues. The major challenge with copper is to ensure its isolation from silicon substrate. Since Cu diffuses rapidly in silicon, and forms deep-level defects, rendering transistors useless, a barrier layer such as tantalum (Ta) or tantalum nitride (TaN) must be deposited first. A passivation layer (cap layer) finishes the isolation. The barrier layer usually has a high resistivity, causing an increase in the effective resistivity of Cu wires (ρ=2.2x 10^{-6} Ω.cm compared to ρ=1.7x 10^{-6} Ω.cm for bulk Cu).

Unlike lift-off Al processes, in which a blanket of Al film is deposited first, and then unwanted portions are etched off, Cu dual damascene processes require a trench or via to be etched first, then a Cu seed layer is deposited after the barrier layer, and then Cu is deposited using electro-chemical deposition (ECD). The result is a different metal line cross sectional area as shown in Fig. 2. The trapezoidal shape with a wider surface makes the resistance modeling less straight forward.

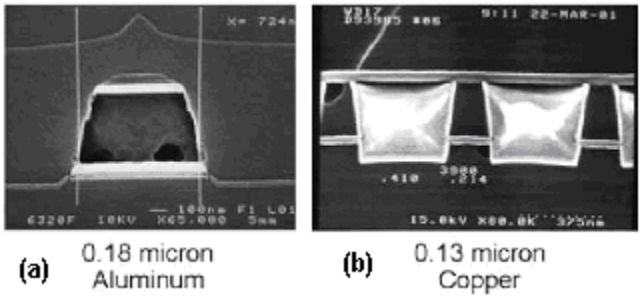

Fig. 2 SEM cross-section of metal lines (a) Al process and (b) Cu process clearly showing CMP dishing effect

The CMP process is important at advanced technology nodes due to the limited depth of focus of advanced lithography. But it also brings effects such as *dishing, and erosion*, which are not known in Al processes [2]. For Cu CMP, Cu is removed selectively, and the removal rate of metal is faster than that of inter-level dielectric (ILD) material, resulting in dishing which refers to the loss of metals in wide lines, and erosion which refers to the loss of dielectric material in between the metal lines where metal density is high. *Dishing and erosion effectively reduce wire thickness locally, and impact on line resistance and capacitance.* The impact on ILD thickness also leads to variations in wire capacitance. In the dual damascene process, the grain size of electro-chemical plated Cu strongly depends on the feature size of lines, resulting in a different resistivity at different line widths. As the line width decreases, the Cu grain size gets smaller, and the mean free path of the electrons becomes shorter, resulting in a higher resistivity (Fig.3). When the metal line widths decrease below 0.2μm, the Cu barrier layer-thinning and surface scattering further increase resistivity. Electron scattering at the surface and grain boundaries needs to be considered in the model for smaller geometries. At wider metal line width (usually larger than 5 μm), dishing occurs and causes the sheet resistance to increase [2].

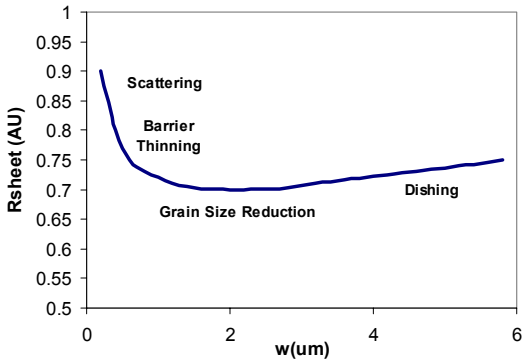

Fig. 3 Cu sheet resistance variation as a function of line width

As a result of both processes (CMP and dual damascene) what is drawn in the design is not what manufactured, Cu line width is *and thickness becomes a function of wire width and spacing, wire pattern density and wire topography*. These new effects must be modeled correctly in order to extract correct parasitic effects.

III. INTERCONNECT MODELING

An interconnect is characterized by three elements, namely, resistance (R), capacitance (C), and inductance (L). Not all of these parameters are equally important. Their relative importance depends upon the length of the line, signal rise time (t_r) driver impedance (Z_s), and line impedance (Z_0) defined as

$$Z_0 = VI = \sqrt{\frac{R + j\omega L}{j\omega C}} \qquad (1)$$

When $Z_s > Z_0$, interconnects can be described by an RC model. However, when $Z_s < Z_0$, inductance effects must be considered and an RCL model is needed.

Historically, interconnect was modeled as a single lumped capacitance using the well known parallel plate capacitance formula. With continued scaling of technology, the wire resistance becomes significant because the wire cross-sectional area decreases while at the same time wire length increases (increased die area). This leads to the development of the RC delay model, first as a lumped RC circuit and then as a distributed RC model (many sections of lumped RC) to improve accuracy. With faster on-chip rise time, higher

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clock frequencies, and use of Cu wires as interconnect, the use of RCL models as a distributed network becomes a necessity. Even more critically, an RCLK model, in which not only self inductance (L), but also mutual coupling inductance (K) is considered, is needed (see Fig. 8). The inclusion of K becomes more important for 90nm technology node and below.

The calculation of R, C, and L matrices of a multi-port, multi-conductor interconnect requires a numerical or field solver approach, which solves Maxwell's electromagnetic field equations, with initial and boundary conditions [8, 9]. The choice of numerical techniques to solve the partial differential equations includes the finite difference method (FD), the finite element method (FE), and the boundary element method (BEM) etc [8, 9]. Both public-domain and commercial tools are available that are based on all these methods [8].

IV. RESISTANCE MODELING

Of the three interconnect parameters, calculation of resistance has been the most straight forward; simply multiply sheet resistance ρ_s by the ratio of length-to-width of the line. However, although this is true for Al wires, it is no longer the case for Cu wires. In fact the resistance of a Cu line is a function of the metal geometry (area and length) and materials properties (resistivity), both of which have been observed to depend on the metal line width, metal pattern density, and metal topography, as discussed previously. Fig. 4 shows the impact of Cu metal density on metal resistivity for various line widths [10].

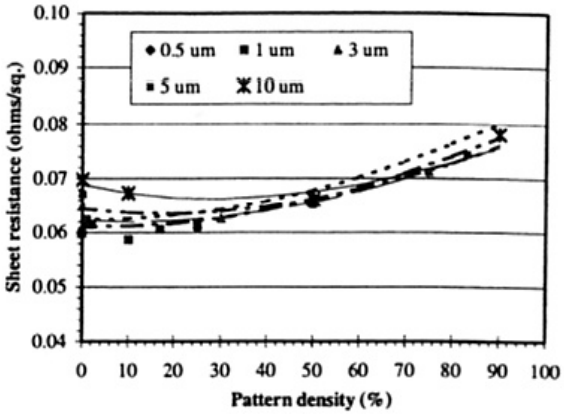

Fig. 4 Resistivity as a function of pattern density and line width (after Zarkesh et al. [10])

Slotting:

CMP process requires slotting in wide lines to prevent dishing. The impact of the slotting can generally be simulated using a 2-D field solver, by calculating current distributions. Table 2 shows resistance of a Cu line calculated using an FEM based 2-D field solver, with and without slotting. This clearly shows the impact of slots on wire resistance.

Table 2: Resistance calculation for the lines shown in Figure 5.

Resistance w/no slots (Ω)	Results with slots (Ω)	Difference No Slots vs. Slots(%)
0.1569	0.1569	0 (a)
	0.1781	13.51 (b)
	0.2340	49.14 (c)

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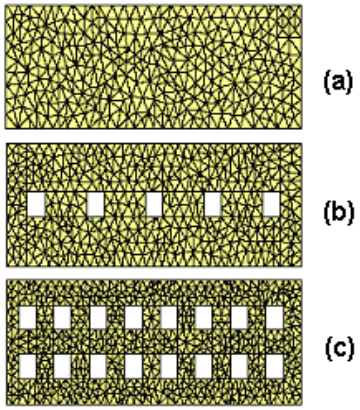

Fig. 5 Resistance modeling using FEM based field solver for metals with slots. Meshing of Cu wire (a) w/o slotting; (b) one row of slotting; (c) two rows of slotting.

At high operating frequency (> 5GHz) skin effect starts to emerge, as the penetrating depth of electromagnetic field decreases, and line resistance increases. The skin depth δ is defined as

$$\delta = 1/\sqrt{\pi f \mu \sigma} \tag{2}$$

where f is the frequency, conductivity and μ is magnetic permeability. For an Al line, the resistance change due skin depth can be described as [11]

$$R = \frac{\rho l}{w\delta\left(1-\exp\left(t/\delta\right)\right)} \tag{3}$$

The frequency dependence of a Cu line in a SoC design is believed to be complicated. The skin depth for a Cu line is around 2μm (vs. 2.8μm for Al) at a frequency of 1GHz; it affects wider lines more than the narrow lines, but it also depends on the surrounding metals and their geometry.

V. CAPACITANCE MODELING

As interconnect scales with each technology generation, the metal wires are getting closer to each other, and the aspect ratio (thickness/width) is increasing. Both aspects of the technology scaling result in an increased coupling capacitance (inter- or intra-level) [5]. Because the aspect ratio of Cu lines is generally smaller than that of Al lines, due to the use of anisotropic low k material, the coupling capacitance of Cu lines is smaller than that of Al lines for the same technology node. However, even for Cu wires coupling starts increasing again with scaling of the devices (see Table 1).

Historically, the capacitances of the wires are modeled using the parallel plate model. This simplified 1D model can no longer be used for today's SoC interconnect due to increasing coupling capacitance which has been ignored in the past. In the 2D modeling approach, all capacitive effects are modeled as a long routing line with per-unit length values. Though more accurate than the 1D model, the 2D model still gives significant errors when calculating two crossing lines, which is a 3D problem [12].

For SoC design, 3D models and field solvers are often used together to extract capacitance based on layout information [8,12]. In general, field solvers can not be used for full-chip RCL extraction, being too compute intensive, and the Monte-Carlo based statistical field solver QuickCap [13] is suitable only for net-by-net analysis in a chip, as it does not involve any meshing. The most commonly used approaches for extracting R and C at the full-chip level are pattern matching using look-up tables, and the even more accurate context-based method that looks at each conductor with in context of its 3D surroundings [14]. The Cadence Fire & Ice® based methodology, which uses a context-based modeling approach, is discussed in reference [12].

As it was pointed out previously, the non-ideal Cu trapezoidal cross-sectional shape also impacts the line capacitance. Consider a signal wire shielded by two neighboring wires, the capacitance of the signal wire consists of self capacitance of the wire to the ground, and the coupling capacitances to the neighboring wires. The self capacitance consists of area and fringe capacitance. In order to describe the non-ideal profile with a non 90 degree vertical angle, a set of effective geometrical parameter are introduced:

$$W(\theta) = 0.5(W + W')$$
$$T(\theta) = T' \qquad (4)$$
$$\frac{1}{S(\theta)} = \frac{1}{S' - S} \ln \frac{S'}{S}$$

where W(θ), T(θ) and S(θ) are derived from the fact that the amount of electric field emission or termination is linearly dependent on the parameters, and the amount of charge induced by the electric field is inversely proportional to S. Capacitances calculated using effective geometrical parameters agree well with results from the field solver for a range of θ from 70° to 100° [15].

Dummy Metal Fill:

In order to reduce dishing and erosion of inter-level dielectrics, CMP requires metal lines to be not too far a distance from each other; in other words certain metal density rule must be satisfied in a given area. This leads to the so-called metal fills (dummy metal), or floating metal lines that are placed statistically in the layout. These dummy metals are of different shapes and sizes, and their impact is to increase line capacitance by 10-18% depending upon shape, size and proximity of the fills to the line [16].

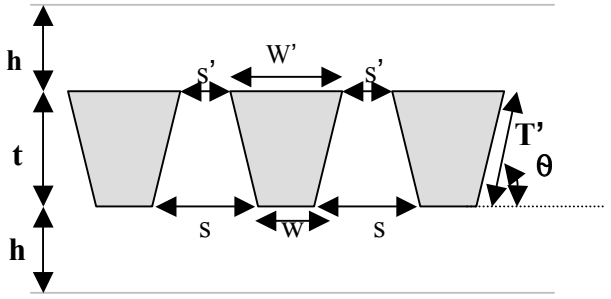

Fig. 6 Effective geometrical parameters for capacitance calculation.

As illustrated by a 2D field simulation, the floating metals cause significant distortion of the electrical field, and thus increase the line capacitance. This capacitance can triple if the adjacent lines are grounded as shown in Figure 7. As such, floating lines should not be grounded while calculating line capacitance (line A in Figure 7).

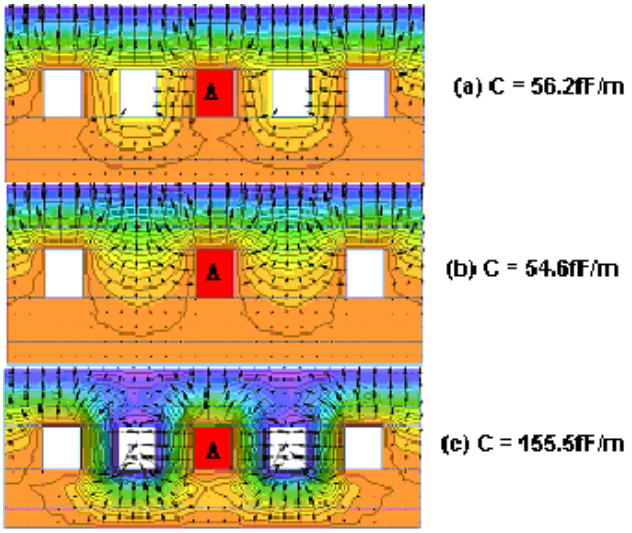

Fig. 7. 2D field simulation of CMP metal fills for line A (a) two surrounding lines (fill) floating; (b) no fills; (c) surrounding lines grounded. If the fill is grounded line capacitance increases three fold.

The coupling capacitance between a signal wire and its neighboring wires increases both delay, which affects the chip frequency, and noise, such as cross-talk, in a chip. Using a three line model, a simplified expression for peak cross-talk voltage is [17]:

$$\frac{V_n}{V_{dd}} = \frac{1}{2}\frac{C_c}{C_c + C_l} = \frac{1}{2}\frac{\frac{1}{ws}}{\frac{1}{tT_{ILD}} + \frac{1}{ws}} \qquad (5)$$

where C_c is the line to line coupling capacitance and C_l is the line to return path capacitance. w and s are line width and spacing, T_{ILD} is the ILD thickness and t is the line thickness.

An SoC consists of a number of heterogeneous mega cells such as control logic, cache memory, arithmetic logic units etc. The wiring bandwidth requirement imposed on SoC global signals, power and clock distribution networks can be

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expressed in terms of wire geometry, by modeling the interconnects as a distributed RC network (a low pass filter) [17],

$$f_{clock} < \frac{1}{2\pi r_{int} c_{int} l^2} = \frac{1}{4\pi\rho\varepsilon\varepsilon_0 \left(\frac{1}{tT_{ILD}} + \frac{1}{ws} \right) A_{SoC}} \quad (6)$$

where r_{int}, c_{int} are the resistance and capacitance of the wire per unit length. It is assumed that global clock distribution is implemented with a balanced H-array, which is approximated as the dimension of the chip A_{SoC}.

The constraint of the clock wiring bandwidth and signal wiring crosstalk noise limit provides a design region of wire thickness and wire width of global SoC interconnect design.

VI. INDUCTANCE MODELING

Since copper has a low resistance, the effect of wire inductance becomes more significant. The contribution of the inductance to the total impedance increases at higher frequency. The inductive effect can cause ringing and overshoot problems in clock lines, and reflections of signals due to impedance mismatch. In addition, switching noise due to inductive voltage drops is an issue for the power distribution network. Figure 8 shows the results of simulation using three different interconnect delay models. Importance of mutual inductive coupling (RLCK model) is evident.

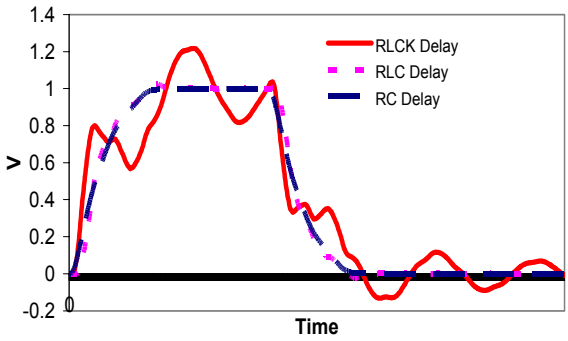

Fig. 8 Signal bus inductive noise simulation using various delay models

Inductance, by definition, is for a loop of wire, the wider the current loop, the higher the inductance. The modeling and calculation of inductance of a wire in an IC requires knowledge of the return path(s). Often, the return path is not easily identified, as it is not necessarily through the silicon substrate. Since magnetic field strength decreases much more slowly compared to electric field strength, unlike capacitance (C) calculation, inductance (L) requires lines to be considered beyond the nearest neighbors, thereby making L calculation more complex at the chip level.

An effective way of analyzing the inductive effect of complex wire structures is the partial inductance (PI) method, in which the structures are broken into simple segments assuming current returns at infinity. The infinite loop cancels out when two segments are subtracted. Based on PI approach, the self and mutual inductances of two parallel lines can be easily calculated using simple analytical formula [18], which is a function of wire length l, width w, thickness t, and separated by distance d.

For wires over a substrate, the return path is through the substrate instead of infinity. The loop inductance of a wire over a ground plane is approximated as[19]

$$L = 0.2 \ln \left(\frac{2\left(h + t/2\right)\pi}{w + t} \right) nH/mm \quad (7)$$

And the mutual inductance of two wires on a ground plane is [18]

$$M = 0.2 \ln \left(1 + \left(\frac{2\left(h + t/2\right)}{D} \right)^2 \right) nH/mm \quad (8)$$

Where h is the wire height from the bottom of the wire to the ground plane. w and t are the width and thickness of metal wire, and D is the center to center wire separation.

Mutual inductance increases monotonically with the spacing between the wire and the nearest ground wire of the coplanar structure. At low frequency, most current returns through the minimum resistance path which often is the nearest ground wire. At higher frequency, current return path is to minimize loop inductance. The inductance is decreased due to proximity effect, which comes from eddy currents which are induced by time-varying magnetic fields. With eddy current, the substrate and even the power grid and random lines can reduce inductance.

Field solver such as FastHenry [20] can be used to extract wire inductance at chip level for critical nets. Figure 9 is a simulation of the inductance vs. frequency of a signal line with multiple coplanar return paths, where w = 0.5um, s = 0.5um and l = 1000um, h = 0.8um. In this figure, the low-frequency inductance value holds up to 1GHz before it starts to decay to a coplanar two-line return (CTR) model. For frequencies up to 1GHz and in the presence of 32 return paths, the actual inductance is more than double that of the CTR model [21].

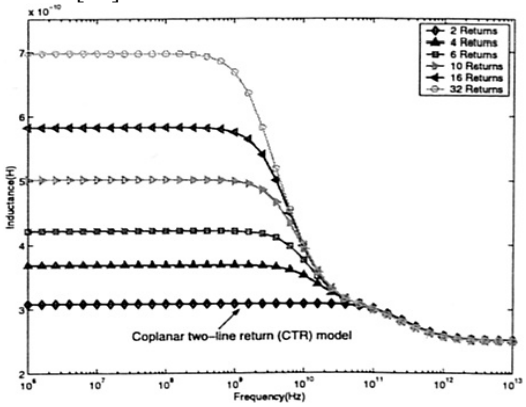

Fig. 9. Inductance vs. frequency using different number of return paths (after Kim et al. [20]).

VII. SILICON VALIDATION

Silicon validation is critical to ensure silicon-accurate interconnect models. Silicon fabricated test structures, though expensive and time consuming, are the only way to verify and silicon validate the models. Interconnect geometry information, as well as material properties could easily be extracted from the test-structure measurement [22].

A resistance model requires an accurate description of the metal width and thickness, as well as sheet resistance variations. Test structures such as Van der Pauw structures and Kelvin structures are often used to extract the Cu sheet resistance, metal line width, and metal thickness at various line width and densities.

The most commonly used test structures for characterizing interconnect capacitance are the so-called passive structures, including parallel plate over a parallel plate, parallel plate over fingers, fingers over a parallel plate, inter-digited fingers, inter-digited fingers over a plate etc. To achieve femto-Farad capacitance measurement, a charge-based capacitance measurement (CBCM) can be used on active test structures [23]. Using this method, the parasitic pad capacitance can be eliminated because CBCM measures the current difference between two nodes connecting to device-under-test (DUT) and reference structure.

High-frequency characterization techniques such as S-parameter measurement are used to characterize and validate inductance model [11, 19].

VIII. CONCLUSIONS

Accurate modeling and characterization of interconnect is essential to SoC design. Cu process and SoC modeling challenges are discussed. A new design approach that reduces wire length, thereby reducing time delay, the so-called X-Architecture, is also briefly discussed. Interconnect characterization, including resistance, capacitance and inductance modeling have been reviewed. Model validations using silicon test chip is briefly covered.

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