Simulation of DGSOI MOSFETs with a Schrödinger-Poisson Based Mobility Model

Andreas Schenk[1] and Andreas Wettstein[2]

[1] Integrated Systems Laboratory, Swiss Fed. Inst. of Technology, Gloriastr. 35, CH-8092 Zürich, Switzerland
e-mail: schenk@iis.ee.ethz.ch, Tel: +41 1 263 6689, Fax +41 1 263 1194
[2] ISE Integrated Systems Engineering AG, Balgriststr. 102, CH-8008 Zürich, Switzerland

I. INTRODUCTION

Ultra-thin DGSOI transistors are considered as one of the most promising devices for future VLSI. Besides expected improvements in the sub-threshold behavior, a theoretical enhancement of the channel mobility was found by some authors. Here, we apply a quantum-mechanical mobility model, based on an integrated Schrödinger/Poisson solver, to double-gate SOI MOSFETs with a range of silicon slab thickness t_{Si} and buried-oxide thickness t_{box}. The main finding is that the theoretical enhancement of effective mobility and on-current at $t_{Si} \approx 10\,nm$ is bound to comparable thicknesses of buried and front oxides. If $t_{box} \approx 100 \times t_{ox}$, as e.g. in the case of SIMOX wafers, the volume-inversion related increase of the mobility completely vanishes.

II. TRANSPORT AND MOBILITY MODEL

The density-gradient model [1], [2] is used in the entire MOSFET which automatically includes the gate quantum-depletion effect [3]. A domain under the front gate covering front oxide, buried oxide, and lowly p-doped ($10^{15}\,cm^{-3}$) silicon slab (see Fig. 1), is subject to the

Fig. 2. Measured [5] versus simulated effective mobility in bulk silicon. Parameters: $t_{ox} = 2\,nm$, $N_A = 10^{15}\,cm^{-3}$, other parameters as given in Table I.

TABLE I
Parameters for the electron mobility. $D_{int,f}$ and $D_{int,g}$ are the inter-valley deformation potential constants for f- and g-type scattering, respectively.

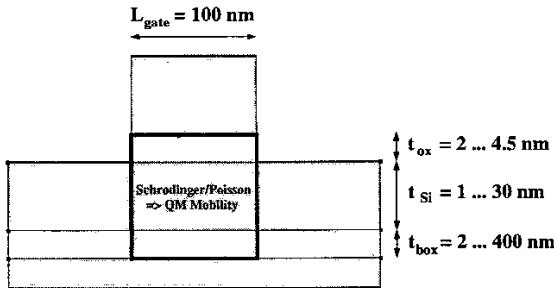| Quantity	Value	Unit
$\Delta_{1,2}$	0.32	nm
$L_{corr\,1,2}$	1.5	nm
α	0.5	$(eV)^{-1}$
$D_{int,g}$	1.0	GeV/cm
$D_{int,f}$	0.2	GeV/cm
D_{ac}/c_l	12	$\mu eVs/cm$
$\hbar\omega_{\nu\nu'}$	60	meV

Fig. 1. DGSOI MOSFET cross section with Schrödinger/Poisson window.

self-consistent Schrödinger/Poisson solver which yields all information (eigenstates, wave functions) needed for the computation of the channel mobility. This 'hybrid' approach has proven to improve convergence at larger drain currents with only little loss of accuracy in the electron density. Details of the density gradient model in the device simulator DESSIS_ISE [4] are described in [1], details of the mobility model can be found in [2]. The
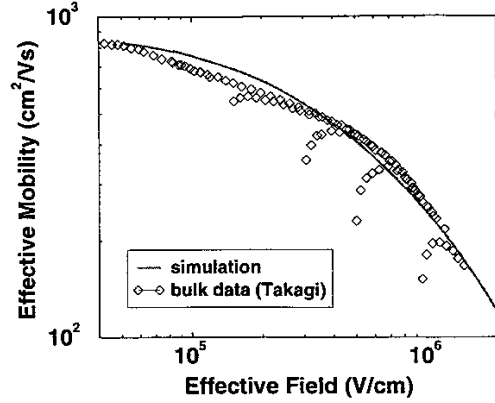
latter makes use of the relaxation time approximation for acoustic-phonon, inter-valley-phonon, and interface-roughness (IR) scattering, but neglects Coulomb scattering, which is negligible in the channel (we focus on the on-state), but is taken into account elsewhere by a conventional default model. Screening of IR scattering is obtained self-consistently by an inner iteration of the system's first-order response to geometrical fluctuations of the interfaces. The number of subbands is restricted to 11 in order to allow for routinely simulations. Bulk coupling constants are used which reproduce the universal mobility curve of bulk MOSFETs (Fig. 2). The parameters used in this paper are summarized in Table I. We assume equal IR amplitudes $\Delta_1 = \Delta_2$ at both interfaces and neglect

the interdependence of upper and lower IR scattering. In particular, the perturbation of the electrostatic potential caused by the displacement of the interfaces is computed separately for the upper and lower interface. The perturbation is assumed to vanish at the top gate and at $z = \infty$ for the top interface, and at the lower gate and $z = -\infty$ for the bottom interface. The modification of the electron density induced by the displacement of the interfaces and the modification of the electrostatic potential is neglected, that is, screening is disregarded. The fit in Fig. 2 was obtained in this way. As shown by Gamiz et al. in Ref. [6] for a simplified IR perturbation Hamiltonian, the modification of the latter due to the presence of the buried interface leads to an increase of the effective mobility in the IR-dominated range compared to the corresponding Hamiltonian used in bulk situations. As in their work the thickness of the buried oxide was large, such a modification will be different for symmetrical DG-SOIs. In the light of the somewhat questionable physical meaning of the commonly used IR perturbation operator and because there are 4 adjustable IR parameters, we did not attempt to follow the line of Ref. [6].
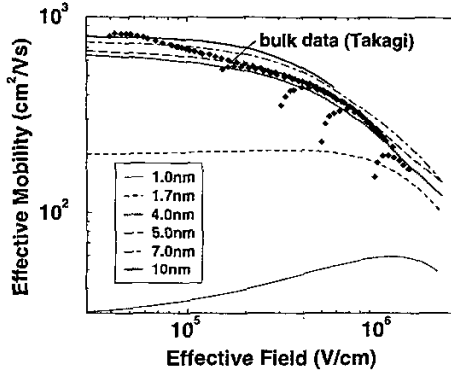

Fig. 3. Effective mobility versus effective field for $t_{ox} = t_{box} = 2\,\mathrm{nm}$, and various t_{Si}. Bulk data [5] are shown for comparison.

The remaining symbols in Table I have the following meaning: $L_{corr\,1,2}$ are the auto-covariance lengths of the roughness fluctuations (assumed to be equal for both interfaces), α is the nonparabolicity parameter, D_{int} and D_{ac} are the inter-valley and acoustic deformation potential constants, respectively, c_l is the longitudinal sound velocity, and $\hbar\omega_{\nu\nu'}$ is the phonon energy involved in inter-valley scattering (Einstein approximation $\hbar\omega_{\nu\nu'} = \hbar\omega_0$ used). The elastic approximation for the acoustic-phonon scattering rate and the equipartition approximation for the acoustic-phonon occupation probabilities have been applied, i.e. $f_B[\vec{q}] \approx k_B T_L/\hbar c_l |\vec{q}|$. Effective mobilities and effective electric fields are computed in analogy to bulk MOSFETs:

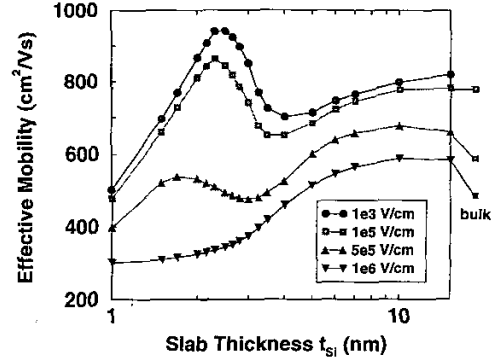$$\mu_{eff} = \frac{\int dz\, \mu[z]\, n[z]}{\int dz\, n[z]} ,$$

Fig. 4. Phonon-limited effective mobility versus SOI thickness for $t_{ox} = t_{box} = 2\,\mathrm{nm}$, and various E_{eff}. IR scattering was switched off.

$$E_{eff} = \frac{\int dz\, |\hat{z} \cdot \vec{E}[z]|\, n[z]}{\int dz\, n[z]} ,$$

where $\hat{z}$ denotes the unit normal vector along quantization direction z, and the interface positions are chosen as integration limits.

III. SIMULATION RESULTS

Fig. 3 shows μ_{eff} versus E_{eff} for the symmetrical DG-SOI ($t_{ox} = t_{box} = 2\,\mathrm{nm}$). In ultra-thin Si films with $t_{Si} < 4\,\mathrm{nm}$ the mobility is suppressed due to geometrical confinement. An enhancement w.r.t. to the bulk curve is observed at intermediate and strong fields around $t_{Si} \approx 10\,\mathrm{nm}$ (compare Fig 2). The phonon-limited effective mobility as function of t_{Si} shown in Fig. 4 serves to explain the behavior in the different t_{Si}-regions in case of the symmetrical DGSOI. The phonon-limited bulk values are reached for $t_{Si} > 15\,\mathrm{nm}$, when the interaction between upper and lower channel gradually disappears due to the growing potential barrier that separates the two inversion layers. The broad maxima around $t_{Si} \approx 10\,\mathrm{nm}$ are caused by the so-called volume inversion. As extensively discussed in Refs. [7], [8], in this region the communication between the two channels is associated with a reduction of the form factors

$$\alpha_{N'N} = \int dz\, |\Psi_{N'}[z]|^2\, |\Psi_N[z]|^2$$

(Ψ_N = envelope of the electron wave function in quantization direction) and, therefore, leads to an enhancement of the mobility compared to the corresponding bulk MOSFET. The latter was obtained from the DGSOI by removing the buried oxide and changing the n^+ back-gate into a p-type substrate. Decreasing the Si thickness, the region governed by geometrical confinement starts at $t_{Si} \approx 4\,\mathrm{nm}$. At low and intermediate effective fields, the mobility first sharply increases, since the average conductivity mass is reduced by the stronger population of the lowest non-primed ladder. With further reduction of t_{Si} the growth of the form factors dominates over sub-band

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splitting and population effects and the mobility sharply drops. However, the range $t_{Si} < 4\,\mathrm{nm}$ is of academic interest only, because it is (currently) inaccessible by technology, and because IR scattering drops the mobility below its bulk values in this region. This is demonstrated in Fig. 5, where IR scattering now is included. As can be
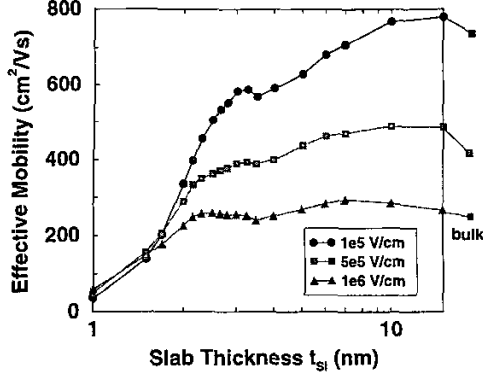

Fig. 5. Effective mobility with IR scattering versus SOI thickness for $t_{ox} = t_{box} = 2\,\mathrm{nm}$, and various E_{eff}.

seen, the mobility enhancement around $t_{Si} = 10\,\mathrm{nm}$ has survived, although reduced in size and at a much lower mobility level. These changes obviously depend on the choice of the IR parameters.

For the mobility enhancement it is essential that two equally filled channels can form. This is impossible in the more realistic case of a thick buried oxide. The results in Fig. 6 for $t_{box} = 200\,\mathrm{nm}$ show that the mobility enhancement vanishes. This case is almost identical to single-gate SOI MOSFETs, where practically no mobility enhancement was found [8].

Fig. 7 compares the symmetrical with the asymmetrical device. For our choice of Δ_2 and L_{corr2}, the difference amounts to 6% at $E_{eff} = 1 \times 10^5\,\mathrm{V/cm}$ and to 15%-16% under strong inversion. These numbers also roughly represent the effect in comparison to the bulk MOSFET.

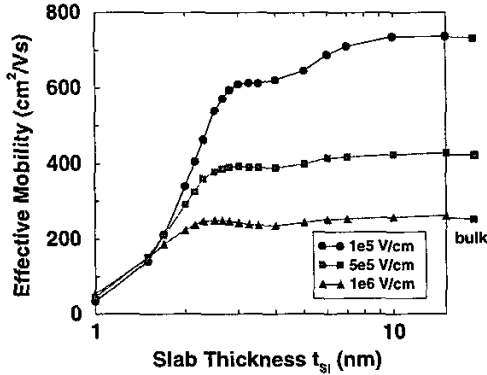The transfer characteristics in Fig. 8 confirm these re-

Fig. 6. Effective mobility with IR scattering versus SOI thickness for $t_{ox} = 2\,\mathrm{nm}$, $t_{box} = 200\,\mathrm{nm}$, and various E_{eff}.
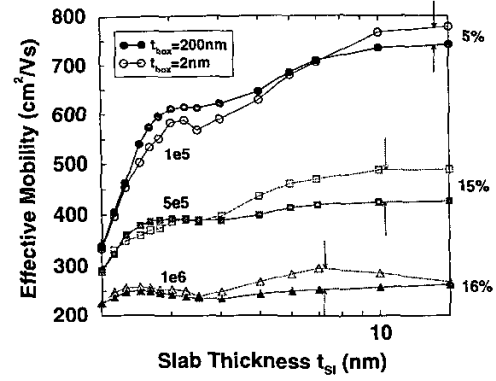

Fig. 7. Effective mobility with IR scattering versus SOI thickness for $t_{ox} = 2\,\mathrm{nm}$ and various E_{eff} and t_{box}.
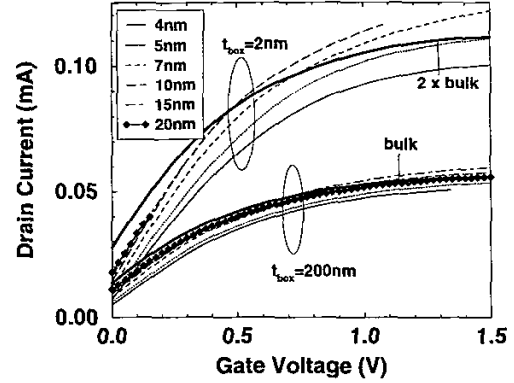

Fig. 8. Transfer characteristics at $V_{DS} = 1\,\mathrm{mV}$ for various t_{Si}.

sults. In the symmetrical case the on-current exceeds two times the current of a bulk MOSFET (two parallel channels!). At $V_{GS} = 1\,\mathrm{V}$ a 8% enhancement on top of that is observed for the 10 nm SOI candidate. However, in the case of $t_{box} = 200\,\mathrm{nm}$ there is only one channel left, and due to the absence of volume inversion the mobility can only gradually approach the bulk value, but not exceed it.

In order to demonstrate the loss of volume inversion with growing buried oxide, we plotted the effective mobility as a function of t_{box} in Fig. 9. An increase of t_{box} by a few nm is sufficient to halve the enhancement. Fig. 10 explains the situation in terms of band edge and density. The density in the upper channel is almost unaffected by an increase of t_{box}, whereas the lower channel vanishes.

A comparison with (rare) experimental data [9]-[11] is shown in Fig. 11. For these simulations, t_{ox} and t_{box} were adapted to the published values. Most striking is the discrepancy for the 5 nm SOI (700 cm^2/Vs simulated versus 420 cm^2/Vs measured), since one would expect the mobility to be phonon-limited in this range. The open circles are very recent data from a sample with 'poor' buried interface [11] (measured density of interface
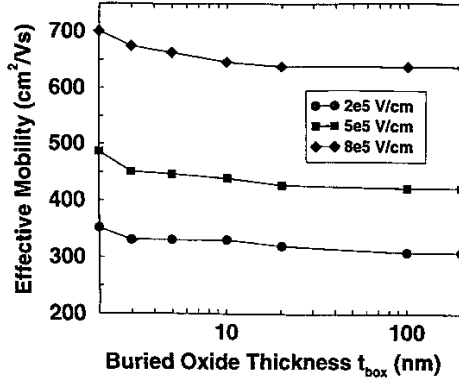
Fig. 9. Decrease of the effective mobility towards its bulk values with increasing t_{box} for various E_{eff} ($t_{Si} = 10\,nm$, $t_{ox} = 2\,nm$).

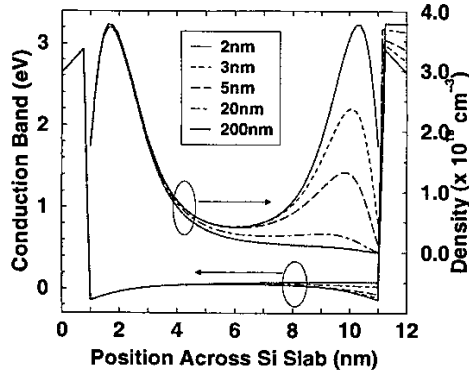Fig. 11. Comparison with experimental data. Parameters: $\Delta_1 = \Delta_2 = 0.32\,nm$.

Fig. 10. Conduction band profile (left) and electron density (right) across the Si slab for various t_{box} ($t_{Si} = 10\,nm$, $t_{ox} = 2\,nm$, $V_{GS} = 1\,V$).

inversion of the buried channel and limit μ_{eff} to the bulk value.

traps $D_{it} = 6 \times 10^{11}\,cm^{-2}eV^{-1}$). For comparison, the same group measured a sample with $t_{Si} = 8\,nm$ (crosses), where the buried interface had a much higher quality ($D_{it} = 4 \times 10^{10}\,cm^{-2}eV^{-1}$). For the same t_{Si}, older data [10] are significantly lower (diamonds). This shows the dramatic influence of the quality of the buried interface on the effective mobility. Koga et al. [11] attributed the mobility degradation in case of the 'poor' buried interface to Coulomb scattering at charged interface states.

IV. CONCLUSION

A quantum-mechanical mobility model based on a 1D Schrödinger-Poisson solver can be routinely used with the device simulator DESSIS$_{-ISE}$. Convergence is improved by a hybrid technique, where the whole device is simulated with the density-gradient model, and only the channel mobility is computed with the information from the Schrödinger-Poisson window. We showed that the volume-inversion related enhancement of μ_{eff} for $t_{Si} \approx 10$ nm is bound to symmetrical DGSOIs. Thick buried oxides, as present in todays SIMOX technology, prevent the

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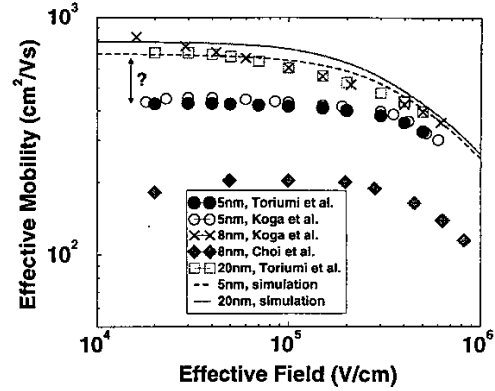[1] O. Penzin A. Wettstein and E. Lyumkis. Integration of the density gradient model into a general purpose device simulator. In press. *VLSI Design*, 2002.

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