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Surface Mobility in Silicon at Large Operating Temperature

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Abstract— In this paper, an experimental investigation on high-temperature carrier mobility in silicon inversion layers is carried out with the aim of improving our understanding of carrier transport at the onset of second breakdown. Special MOSFET structures suitable for Hall measurements were designed and manufactured using the BCD-3 technology available at ST-Microelectronics. Hall measurements were carried out using a special measurement setup that allows operating temperatures in excess of 400°C to be reached within the polar expansions of a commercial magnet. A novel extraction methodology allowing for the determination of the Hall factor and the carrier mobility against impurity concentration and lattice temperature was devised. Finally, a compact mobility model suitable for implementation in device simulators has been worked out, implemented in the DESSIS© code and validated within an industrial environment.

I. INTRODUCTION

In this study we investigate carrier mobility in MOSFETs at large operating temperature with the aim to improve our understanding of second breakdown and thermal runaway, which can occur in silicon devices under high-voltage and high-current conditions. This goal has been pursued within the context of a European project called ESDEM and, subsequently, a German research project called PARASITICS. In order to reliably predict by numerical simulation the occurrence of second breakdown, it was felt that the existing models of impact ionization and carrier mobility had to be extended and validated up to at least 400°C. This paper specifically addresses the issue of surface mobility, which has been measured from specially-designed test structures in the temperature range between 25 and 400°C. Furthermore, a new mobility model suitable for implementation in simulation codes has been worked out and validated in the above temperature range. The model is based on, and improves upon, previous works by Schwarz and Russek [1], Lombardi *et al.* [2] and Darwish *et al.* [3]. In a previous paper, the silicon bulk mobility was investigated [4]. Its expression represents the starting point for the present development, which heavily relies on the experimental contribution by Takagi *et al.* [5].
This work was carried out in close cooperation by four Institutions, namely: ST-Microelectronics designed and manufactured the required test structures using the BCD-3 smart-power technology; ETHZ conceived, realized and tested the experimental setup and carried out the high-temperature measurements; the University of Bologna performed the extraction of the carrier mobility from experimental data and worked out a new compact mobility model which holds from 25 to 400°C; finally, Bosch validated the model by simulation of the test structures and comparison of simulated and experimental data.
Carrier mobility has been determined from conductance and Hall measurements carried out at ETHZ on special MOSFET structures with lateral contacts along the channel. In order to extend the temperature range of the measurements, a novel experimental setup has been devised which allows us to controllably heat up the device under test (DUT) within the polar expansions of a magnet. This is achieved by means of a dedicated sample holder which, besides offering up to 10 electrical contacts to the DUT, has provisions for a microcomputer-controlled heating system.
A new mobility-extraction methodology from resistivity and Hall measurements has been developed which does not require any assumption on the specific values of the Hall factor. Rather, the latter is determined from the experimental mobility behavior against doping and temperature.
This paper is organized as follows: in the next section we discuss the test structures designed for mobility measurements. Section III addresses the problem of high-temperature measurements and illustrates the setup which allows for a uniform heating of the sample within the polar expansion of a magnet. Section IV presents the compact mobility model proposed in this paper, which holds for temperatures ranging between 20 and 400°C, and compares it with literature data and with previous models. Section V illustrates the measurement results and the methodology used to separately extract both surface mobility and Hall factor against doping and temperature. Conclusions are drawn in Section VI.

II. STRUCTURE FABRICATION

Special test structures were designed and fabricated with the purpose of carrying out the high-temperature measurements. More specifically, long-channel devices were designed with lateral contacts on both sides of the channel, as shown in figure 1, in order to make Hall measurements feasible. The Hall technique allowed us to measure the carrier density per unit area within the MOSFET channel with a supposedly-small uncertainty due to the Hall factor. Four different MOSFETs were fabricated in the test chip using suitable n and p layers made available by the BCD-3 technology.

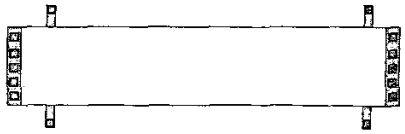

Figure 1. Layout view of the MOSFET structure for Hall measurements.

The first set of MOS transistors is characterized by a 170 μm gate length, 42.5 μm width and 25.5 nm oxide thickness. In the following, they are referred to as the N-HALL and P-HALL devices. The N-HALL transistor was fabricated in a p-well diffusion on an n-epi layer, with channel implantation. The surface doping density is about 3×10^{16} cm^{-3}. The P-HALL transistor was directly fabricated in the n-epi layer, with channel implantation. The surface impurity concentration is about 4×10^{16}cm^{-3}. The gate bias can nominally reach 5 V, but experiments were carried out for biases up to 20 V. N-HALL and P-HALL devices have been measured at temperatures up to 625 K.

The second set of MOSFETs is characterized by 100 μm gate length, 20 μm width and 40 nm oxide thickness. In the following, they are referred to as the NMOS and PMOS devices. Both of them were fabricated without any channel implant and the doping density at the Si-SiO_2 interface is about 2.9×10^{16} cm^{-3} in the NMOS and 3.2×10^{15} cm^{-3} in the PMOS devices. In this case, the gate bias can nominally reach 11-12 V, but data measurements were collected for biases up to 20 V. NMOS and PMOS devices were measured at temperatures below 675 K.

It has been found that the n-epi/p-well junction in the n-channel devices and, correspondingly, the p-substrate/n-epi junction in the p-channel devices influence the measurement results due to carrier generation, which becomes more and more important as temperature increases. In order to collect thermally-generated carriers at the body and epi (or substrate) contacts, the junctions have been kept reverse-biased at $\pm$ 2.5 V.

III. MEASUREMENT SETUP

The Hall technique was chosen in order to have an independent determination of the inversion-layer charge. The requirement of measuring Hall mobility at temperatures up to 4o0°C made the development of a custom measurement setup necessary. Details about its main features were given in [4]. The Hall measurement system is a temperature-controlled apparatus with DUT-mounting facilities and automated instrument control. For the Hall measurements, the drain current was adjusted while changing the gate voltage up to 20 V in order to keep the drain voltage low enough to ensure a negligible perturbation of the channel. The magnetic field has been fixed to 0.7 Tesla. The measurement apparatus provides two distinct parameter values for each bias: the "transverse" resistance, R_t, and the MOSFET resistance, R_ρ. The transverse resistance is the ratio between the Hall voltage V_H, and the drain current I_D; the MOSFET resistance is instead the ratio between the drain-source voltage and the drain current at low V_{DS}. With the new extraction methodology, to be described in section V, both the Hall factor and surface mobility have been determined consistently with the measured data.

IV. ELECTRON- AND HOLE-MOBILITY MODELS

According to the classical semiconductor equations implemented in general-purpose device simulators, the inversion-layer mobility within the channel is locally defined against the transverse electric field. The local function $\mu(E_\perp, N_i, \text{bulk})$ has been chosen as a physically-based semi-empirical model with a number of parameters fitted to give the best agreement with experiments. Moreover, this model is applicable not only within the MOSFET inversion layer, but anywhere within the device. Starting from the bulk mobility [4], a number of contributions have been added, each corresponding to a different surface scattering mechanism. More specifically, the model includes phonon, Coulomb and surface-roughness scattering, which are modeled as functions of local quantities only, using Matthiessen's rule. Next, the effective carrier mobility is accurately computed and compared with experimental mobility data against effective normal field in order to reproduce the universality of the electron and hole mobility curves.

To extract the functional dependence of carrier mobility on excess carrier concentration and normal electric field, the effective mobility was numerically computed by integration over the channel depth using established semiconductor device equations. The effective carrier mobility is expressed as

$$\mu_{\text{eff}} = \frac{q}{Q_i} \int_0^{x_b} N_i(x)\mu(x)dx\,, \qquad (1)$$

where x_b is the space-charge width, $N_i = n(x) - n_0$ is the excess minority carrier concentration per unit volume in the inversion layer, Q_i is the inversion-layer charge density and $\mu(x)$ is the local mobility function we want to model. In order to work out a local model independent of the device geometry, the x dependence of mobility was assumed to be due to its direct dependence on impurity concentration, N_i and $E_\perp$.

By accounting for screened Coulomb scattering, the present model very well predicts the roll-off of effective mobility in the low field region for a wide range of doping concentrations. Finally, the model was calibrated to properly account for temperature changes.

A. Analytical model description

The Matthiessen-like mobility function we used reads

$$\frac{1}{\mu(E_\perp, N_i, \text{bulk})} = \frac{1}{\mu_{\text{bsc}}} + \frac{1}{\mu_{\text{sph}}} + \frac{1}{\mu_{\text{sr}}}\,. \qquad (2)$$

The μ_{bsc} term is associated to the substrate impurity and carrier concentrations. It is decomposed into an unscreened part, due to the impurities, and a screened part related to the local excess carrier concentration:

$$\mu_{\text{bsc}} = \mu_b(1 + f_{\text{sc}}^\tau)^{1/\tau}\,, \qquad (3)$$

where μ_b is the bulk mobility model presented in [4] and τ is a parameter equal to 1 for electrons and 3 for holes.

The screening function is given by

$$f_{sc} = \left(\frac{N_1}{N_A + N_D}\right)^r \frac{N_i}{N_A + N_D}. \quad (4)$$

Eq. (3) correctly models the roll-off in the effective mobility curves. As the effective field increases, mobility becomes independent of the channel doping and approaches the universal curve. The main scattering processes are surface-phonon and surface-roughness scattering, namely

$$\mu_{sph} = A\left(\frac{N_{sub}}{N_2}\right)^a \frac{1}{E_\perp^\delta}, \quad (5)$$

$$\mu_{sr} = B\left(\frac{N_{sub} + N_3}{N_4}\right)^b \frac{1}{E_\perp^\lambda}. \quad (6)$$

No dependence on doping or carrier concentration appears in the field exponent in (6), as proposed by [3]. An optimized set of values for the fitting parameters in eqs. (4), (5) and (6) are shown in tables I and II for electrons and holes, respectively ($T_n = T/300$).

Parameters	Electrons
N_1 (cm^{-3})	$2.34 \cdot 10^{16}$
N_2 (cm^{-3})	$4.0 \cdot 10^{15}$
N_3 (cm^{-3})	$1.0 \cdot 10^{17}$
N_4 (cm^{-3})	$2.4 \cdot 10^{18}$
A (cm^2/Vsec)	$1.86 \cdot 10^4 \cdot T_n^{-1.68}$
B (cm^2/Vsec)	$5.8 \cdot 10^{18}$
τ	1
r	0.3
a	0.026
b	0.11
δ	0.29
λ	2.64

TABLE I
SURFACE MOBILITY PARAMETERS FOR ELECTRONS

Parameters	Holes
N_1 (cm^{-3})	$2.02 \cdot 10^{16}$
N_2 (cm^{-3})	$7.8 \cdot 10^{15}$
N_3 (cm^{-3})	$2.0 \cdot 10^{15}$
N_4 (cm^{-3})	$6.6 \cdot 10^{17}$
A (cm^2/Vsec)	$5.726 \cdot 10^3 \cdot T_n^{-1.3}$
B (cm^2/Vsec)	$7.82 \cdot 10^{15} \cdot T_n^{1.4}$
τ	3
r	0.5
a	−0.02
b	0.08
δ	0.3
λ	2.24

TABLE II
SURFACE MOBILITY PARAMETERS FOR HOLES

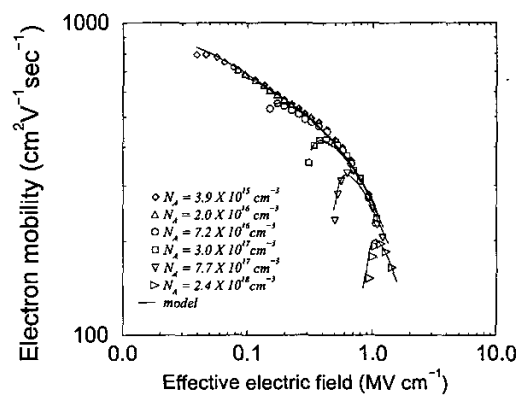

Figure 2. Electron mobility curves in MOSFET inversion layers for various impurity concentrations. Experiments are from [5]. The effective electric field has been computed with $\eta = 0.5$.

B. Calibration of the surface mobility

The first mobility calibration was carried out using the experimental data by Takagi [5], whose measurements were carried out on long-channel n-MOS and p-MOS transistors with a homogeneous substrate concentration. In order to calibrate the model on experimental data, a number of simulations were performed for long-channel n-MOS and p-MOS transistors following the suggestions given in [5]. Then, the effective mobility was numerically computed by integration over the channel depth using established semiconductor-device equations and the surface potential provided by the solution of Poisson's equation. The effective normal field was computed as

$$E_{eff} = (Q_b + \eta Q_i)/\varepsilon_s, \quad (7)$$

where Q_b is the depletion-region charge density, Q_i is the inversion-layer charge density and ε_s is the silicon dielectric constant. The value of η is 0.5 for electrons, which gives the true average normal field, and 0.3 for holes, which provides an optimal universal relationship. Figs. 2 and 3 compare the electron and hole effective mobility models with Takagi's experimental data for different substrate doping concentrations. The agreement is good over the whole range of effective-fields and substrate dopings. By accounting for the screened Coulomb scattering, the present model nicely predicts the roll-off of effective mobility in the low field region for a wide range of doping concentrations. Figs. 4 and 5 represent the universal curves of electron and hole effective mobilities, respectively, for temperatures ranging from 242 to 447 K for electrons, and from 223 to 443 K for holes. A good agreement has been found even below room temperature, notwithstanding the lack of model calibration in this region.

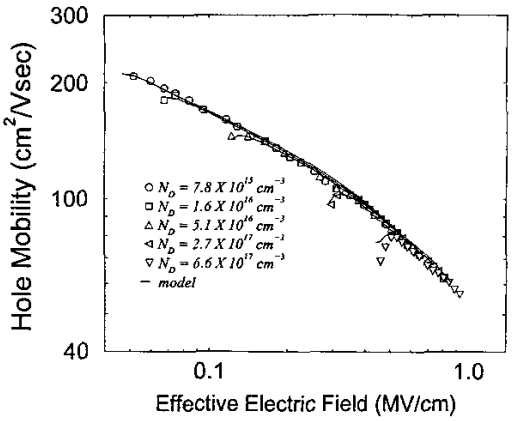

Figure 3. Hole mobility curves in MOSFET inversion layers for various impurity concentrations. Experiments are from [5]. The effective electric field has been computed with $\eta = 0.3$.

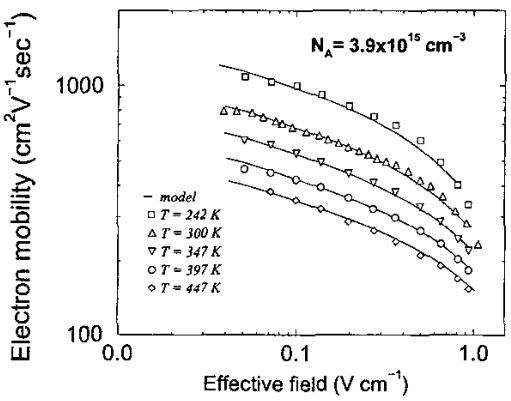

Figure 4. Universal electron mobility curves in MOSFET inversion layers for different lattice temperatures. Experiments are from [5]. The effective normal field is computed with $\eta = 0.5$.

V. EXPERIMENTAL RESULTS

A. Extraction of the Hall factor

The Hall measurement system described in section III can be configured to measure both the MOSFET resistance R_ρ and the Hall coefficient R_H. Hence, Hall mobility and Hall inversion-layer charge can be inferred. Their expressions are worked out as follows. The Hall coefficient R_H is given by

$$R_H = \frac{V_H}{BI_D} = \frac{a_H}{qN_{inv}}, \tag{8}$$

where a_H is the Hall factor, and N_{inv} is the carrier density per unit area.

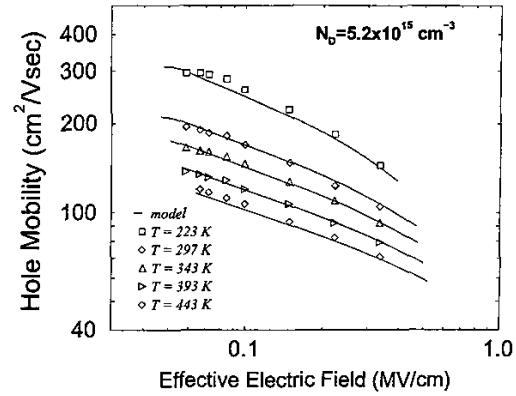

Figure 5. Universal hole mobility curves in MOSFET inversion layers for different lattice temperatures. Experiments are from [5]. The effective normal field is computed with $\eta = 0.3$.

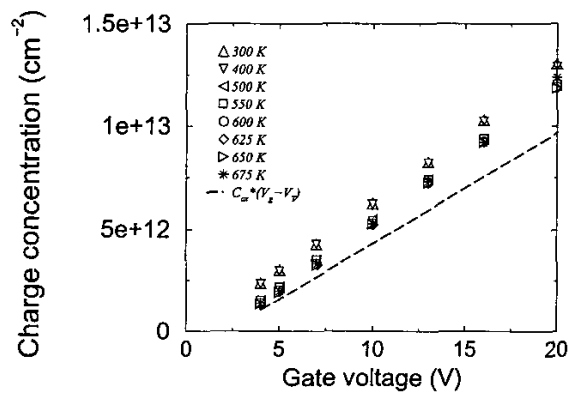

Figure 6. Hall charge density (electrons) per unit area N_{inv}/a_H vs gate voltage at temperatures ranging from 300 to 675 K (NMOS device). Symbols represent $1/qR_H$ values. The dashed line shows the charge density from eq. (12).

The sheet resistance $R_\square$ is defined as

$$R_\square = R_\rho \frac{W}{L} = \frac{1}{q\mu N_{inv}} = \frac{R_H}{a_H \mu}. \tag{9}$$

The Hall mobility is given by the following expression

$$\mu_H = a_H \mu = \frac{R_H}{R_\square} \tag{10}$$

and the Hall inversion-layer charge Q_{iH} reads

$$Q_{iH} = \frac{Q_i}{a_H} = \frac{qN_{inv}}{a_H} = \frac{1}{R_H}. \tag{11}$$

Both the Hall mobility and the Hall inversion-layer

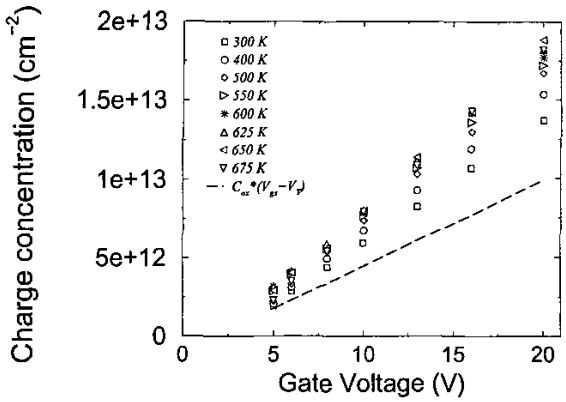

Figure 7. Hall charge density (holes) per unit area N_{inv}/a_H vs gate voltage at temperatures ranging from 300 to 675 K (PMOS device). Symbols represent $1/qR_H$ values. The dashed line shows the charge density from eq. (12).

charge can thus be computed from geometrical and measured quantities. The extraction of the conductivity mobility and of the real inversion-layer charge requires the Hall factor to be known against doping and temperature, but literature data are controversial for bulk silicon [4], [8], and largely missing for inversion layers. Otherwise, an independent determination of the inversion-layer charge is needed. MOSFET simulations indicate that, for a given gate voltage, the inversion-layer charge is remarkably independent of lattice temperature. Thus, the following expression

$$N_i = \frac{1}{q} C_{ox}(V_{GS} - V_T)\,, \qquad (12)$$

which holds for a MOSFET biased in strong inversion, can be used. The Hall factor a_H is thus determined as the ratio between the slope of (12) given by C_{ox}/q and the slope of the regression lines extracted from the experimental data for each set of measurements at every temperature. This gives $a_H = N_i/N_{iH}$ as a function of temperature.

The experimental Hall charge concentrations are reported in Figs. 6 and 7 for the NMOS and PMOS devices, respectively, and compared with eq. (12) (dotted line). The extracted Hall factors are reported in Fig. 8 as a function of temperature for all measured devices. It can be seen that the Hall factor for holes exhibits a stronger temperature dependence than the Hall factor for electrons, which is nearly uniform vs temperature and equal to about 0.85. Starting from a simplified semiconductor model, with single-valley conduction and valence bands having spherical isoenergetic surfaces, the analytical calculation of the Hall factor gives $a_H = 3\pi/8 \simeq 1.18$ for both electrons and holes [6]. A more accurate theory accounting for the multi valley conduction band of silicon and the degeneracy of the valence band is reported in e.g. [7]. For bulk silicon it turns out that $a_{Hn} \simeq 1.02$ and $a_{Hp} \simeq 1.57$. Thus, the discrepancy with our data is especially striking for holes, the Hall factor of which ranges between 0.7 and 0.5 as temperature varies from 300 to 675 K.

Simulations of the Hall effect in MOSFET inversion layers were carried out by Jungemann *et al.* [9]. Their model accounts for a 2-D electron gas and accounts for the most important physical effects occurring in silicon inversion layers, including multisubband carrier transport, surface-phonons and surface-roughness scattering. They find a weak dependence of the Hall factor upon the effective normal field from 200 to 500 K and values slightly larger than one for most impurity concentrations. No simulation for holes was carried out by the above authors.

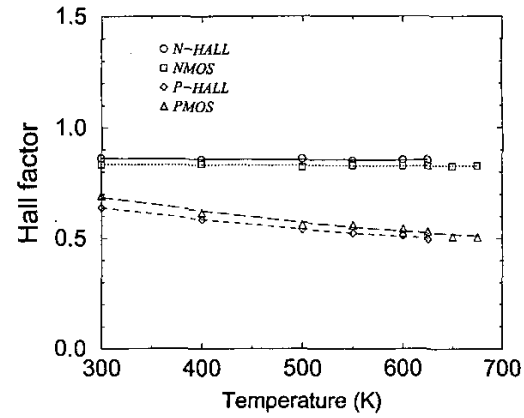

Figure 8. Hall factor vs temperature for both electrons and holes. Continuous lines show the quadratic-regression fitting on the extracted data.

B. Effective mobility results

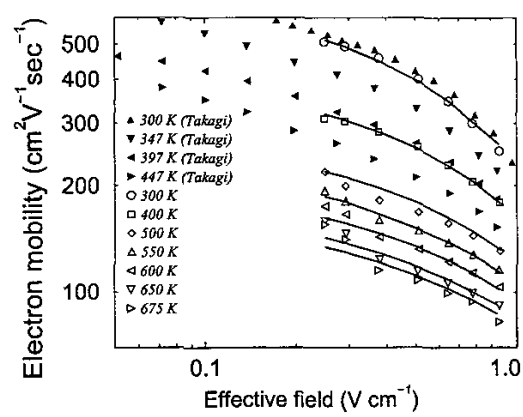

Figure 9. Effective electron mobility vs gate voltage at different temperatures (NMOS device). Symbols show the Hall measurement results. Continuous lines show the model results.

A number of simulations were carried out to validate the surface mobility model on the new experiments.

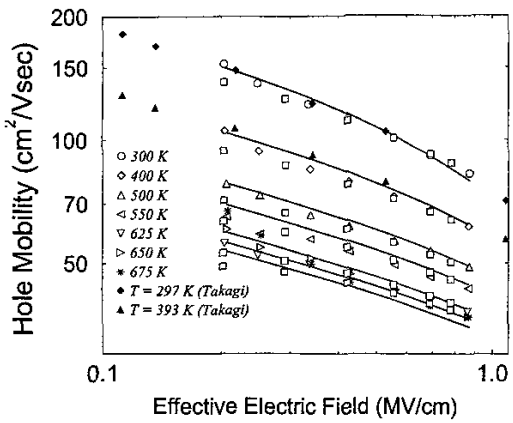

Figure 10. Effective hole mobility vs gate voltage at different temperatures (PMOS device). Symbols show the Hall measurement results. Continuous lines show the model results.

First, the model described in the previous section was implemented in the DESSIS© code. Process and device simulation were then used to generate the structure of the measured devices and compute their electrical characteristics. So doing, realistic doping profiles were taken into account in the validation procedure. The mobility data were extracted from the MOSFET turn-on characteristics at low V_{DS} after integration of the channel charge.

The simulated electron and hole effective mobilities (solid lines) are compared in Figs. 9 and 10 with our experimental data. The agreement is good over the explored range of effective normal fields and temperatures. For comparison, Takagi's data [5], which extend deeper into the low-field region but only cover a temperature range below 447 and 393 K for electrons and holes, respectively, are reported in the same figures. The agreement between the simulated effective mobilities and the experimental data indicates that the local mobility model implemented in the DESSIS© code can be reliably used in numerical device simulation over an extended temperature range.

VI. CONCLUSIONS

In this work n- and p-type long-channel MOSFETs were fabricated in order to investigate the inversion-layer electron and hole mobilities at large lattice temperatures. The experimental study was based on Hall measurements up to 400°C. A new measurement setup for device characterization has been designed, installed and automated, and a large number of measurements covering the temperature range between 300 and 675 K have been carried out.

A TCAD-oriented carrier mobility model in silicon inversion layers is presented which is especially suitable for implementation in device simulators. The effects of transverse electric field, temperature, and impurity concentration are fully accounted for. Starting from bulk mobility, the surface mobility model has been worked out by adding the carrier-screening, surface-phonons and surface-roughness contributions. The model has been tested by a number of simulations of long-channel MOSFETs and turns out to hold in a wide temperature range between 300 and 675 K. We hope that such a model will help improve our understanding of second breakdown and current filamentation, which occurs in silicon devices under extreme bias conditions.

Furthermore, an unprecedented experimental determination of the Hall factor in MOSFET inversion layers against temperature and doping density has been carried out. The Hall factor turns out to be consistently smaller than 1 and exhibits a negligible temperature dependence for electrons, while it decreases with temperature for holes with no saturation effect up to 700 K.

ACKNOWLEDGMENTS

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