Numerical Modeling of Impact-Ionization Effects on Gate-Lag Phenomena in GaAs MESFETs

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Abstract

Two-dimensional simulation of turn-on characteristics of GaAs MESFETs is performed in which surface states and impact ionization of carriers are considered. It is shown that the gate-lag (or the slow current transient) becomes weaker when including the impact ionization. This is attributed to the fact that the potential profiles along the surface is drastically changed when the surface states capture holes that are generated by impact ionization. The relation between the gate-lag and the so-called kink phenomenon is also discussed.

1 Introduction

The gate-lag in GaAs MESFETs is a phenomenon that the drain current shows slow transient even if the gate voltage is changed abruptly. This is a serious problem in digital radio systems that are pulsed on and off with short duty cycle. This phenomenon is also known to degrade the distortion characteristics. As for the mechanism of gate-lag, effects of surface states are suggested, but the detailed mechanism is not well understood [1],[2].

To understand high-voltage phenomena in GaAs MESFETs, such as drain-to-source breakdown, is also important for realizing high-performance microwave power devices and ICs. In relation to this, recently, an abnormal increase in output conductance with the drain voltage ("kink") was often observed at relatively low-voltage regions. Since the kink in GaAs MESFETs was firstly correlated to a sidegating effect, the kink was discussed in terms of substrate-related effects [3],[4]. However, the surface-related factors, such as the existence of surface states, should also affect the breakdown and the kink phenomena. Nevertheless, few works have been reported on how the surface properties affect the kink phenomena in GaAs MESFETs [5].

In this work, we have made two-dimensional simulation of GaAs MESFETs, in which surface states and impact ionization of carriers are considered, and studied how the surface states affect the gate-lag and the kink phenomena. Particularly, we discuss how the gate-lag is influenced by impact ionization of carriers.

2 Physical model

A simplified planar structure is mainly analyzed here, although a recessed-gate structure is also treated. The surface states are considered on the planes between source and gate and on the planes between gate and drain. As for a surface-state model, we

adopt Spicer's unified defect model [6], and assume that the surface states consist of a pair of a deep donor and a deep acceptor. As to their energy levels, we consider the following case based on experiments, as in previous works [1],[5]: $E_{SD} = 0.87$ eV, $E_{SA} = 0.7$ eV [7]. Here E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. The surface states are assumed to distribute uniformly with 5 Å from the surface and their densities (N_{SD}, N_{SA}) are typically set to $2\text{x}10^{20}$ cm^{-3} (10^{13} cm^{-2}). According to a previous work [1] where impact ionization is not included, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap in this case.

Basic equations to be solved are expressed as follows.

(a) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A + N_{SD}^{+} - N_{SA}^{-}) \tag{1}$$

(b) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n + G - (R_{n,SD} + R_{n,SA}) \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p + G - (R_{p,SD} + R_{p,SA}) \tag{3}$$

$$G = (\alpha_n \mid J_n \mid + \alpha_p \mid J_p \mid)/q \tag{4}$$

$$R_{n,SD} = C_{n,SD} N_{SD}^{+} n - e_{n,SD}(N_{SD} - N_{SD}^{+}) \tag{5}$$

$$R_{n,SA} = C_{n,SA}(N_{SA} - N_{SA}^{-})n - e_{n,SA} N_{SA}^{-} \tag{6}$$

$$R_{p,SD} = C_{p,SD}(N_{SD} - N_{SD}^{+})p - e_{p,SD} N_{SD}^{+} \tag{7}$$

$$R_{p,SA} = C_{p,SA} N_{SA}^{-} p - e_{p,SA}(N_{SA} - N_{SA}^{-}) \tag{8}$$

(c) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{SD} - N_{SD}^{+}) = R_{n,SD} - R_{p,SD} \tag{9}$$

$$\frac{\partial}{\partial t} N_{SA}^{-} = R_{n,SA} - R_{p,SA} \tag{10}$$

where N_{SD}^{+} and N_{SA}^{-} represent ionized densities of the deep donors and the deep acceptors, respectively. α_n and α_p are ionization rates for electrons and holes, respectively, and are taken from [8]. C_n and C_p are the electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are the electron and hole emission rates of the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level [1]. The other symbols have their normal meanings. These equations are put into discrete forms and are solved numerically.

3 Calculated results and discussions

Fig.1 shows a comparison of calculated turn-on characteristics of a GaAs MESFET with and without impact ionization. Even if the gate voltage is switched on, the drain current remains a low value for some periods and begins to increase slowly, showing large gate-lag. The gate-lag is smaller for the case with impact ionization. This can be understood from the potential profiles shown in Fig.2. As seen in Fig.2(a), without impact ionization, the drain voltage is entirely applied along the interface between drain electrode and surface-state layer in this hole-trap case [1], and the ionized deep-acceptor density N_{SA}^{--} increases in this region because of hole depletion. On the other hand, in the case with impact ionization, generated holes at the drain edge are captured by the deep acceptors, resulting in the decrease in N_{SA}^{--} there, and hence the potentials become applied along the surface-state layer between gate and drain electrodes (Fig.2(b)). Therefore, in the OFF state, the electron depletion under the surface-state layer is weaker for the case with impact ionization, resulting in the smaller gate-lag. It is experimentally suggested that the gate-lag becomes weakened in the high-voltage region where carrier generation becomes important [9].

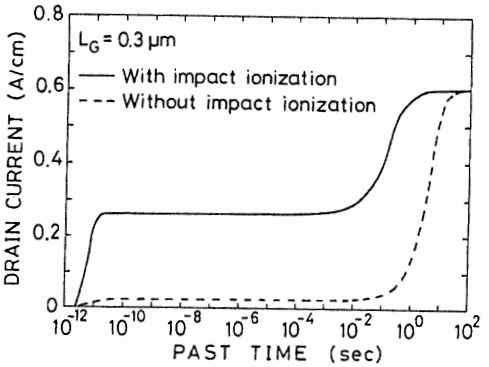

Fig.1. Comparison of calculated turn-on characteristics of GaAs MESFET with and without impact ionization. The surface-state densities are $2x10^{20}$ cm^{-3}.

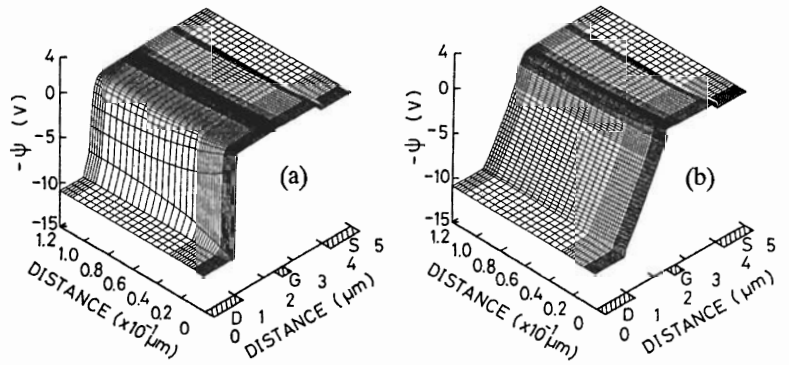

Fig.2. Comparison of potential profiles of GaAs MESFET (a) without and (b) with impact ionization.

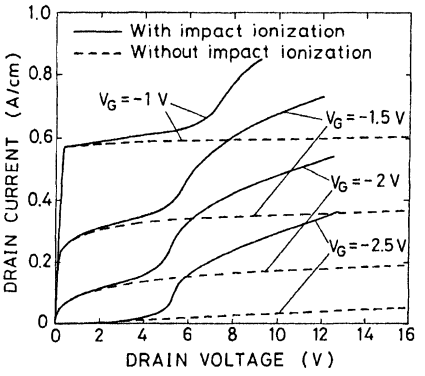

Fig.3. Calculated I_D-V_D characteristics of GaAs MESFET with surface-state densities of $4x10^{19}$ cm^{-3}.

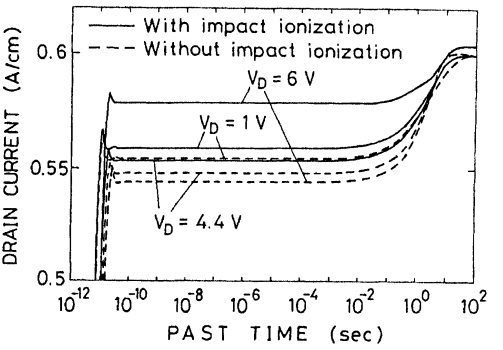

Fig.4. Calculated turn-on characteristics of GaAs MESFET as a parameter of the drain voltage V_D, corresponding to Fig.3.

Next, we describe a case with lower surface-state densities of $4x10^{19}$ cm^{-3} ($2x10^{12}$ cm^{-2}). Fig.3 shows a comparison of calculated drain characteristics of the GaAs MESFET with and without impact ionization. With impact ionization, the drain currents begin to increase steeply around V_D = 5 V, showing the kink behavior. It is understood that the kink occurs because holes are generated by impact ionization and are captured by the surface states, and hence the net negative charges at the surface decrease, leading to widening the channel thickness. Fig.4 shows the calculated turn-on characteristics as a parameter of the drain voltage V_D. Without impact ionization, the gate-lag becomes slightly larger for higher V_D. But, with impact ionization, the gate-lag becomes rather small at V_D = 6 V where the impact ionization becomes important. This is also understood from the fact that the potential profiles along the surface are influenced by impact ionization of holes and the following hole trapping by the surface states.

4 Conclusion

Effects of impact ionization of carriers (together with surface states) on the gate-lag and the kink phenomena in GaAs MESFETs are studied by two-dimensional simulation. It has been shown that the gate-lag becomes smaller when the impact ionization becomes important --- which is consistent with experiments, because the potential profiles along the surface are strongly influenced by the surface states' hole capturing.

References

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