An Effective Methodology for Predicting the Distribution of MOSFET Device Characteristics Using Statistical TCAD Simulations

Takaaki Tatsumi
LSI Technology Development Division,
Semiconductor Network Company, Sony Corporation
4-14-1, Asahi-cho, Atsugi-shi, Kanagawa-ken, Japan
tatsumi@ulsi.sony.co.jp Tel:+81-46-230-5719 Fax:+81-46-230-5945

Abstract

We have developed a novel and effective method for predicting the distribution of MOSFET device characteristics, which also enables us to specify the most typical process conditions for any device characteristics. In our approach, the distribution of the device characteristic caused by the fluctuation of every single process are calculated and then merged. Comparison with the result of the measured data has established that our method is accurate and practical.

1. Background

Predicting accurate distributions of device characteristics using TCAD at the device development phase is indispensable for the concurrent designing of cell libraries and circuits with appropriate performance margins. While designing, the saturated drain current of NMOS and PMOS (IdsN and IdsP) pair is used as the reference of the best/worst performance conditions. By measuring the IdsN-IdsP pairs of manufactured chips, it has been found that their distribution assumes an oval shape, as shown in Fig.1. Process conditions which lead to particular device characteristics, the FF and SS points in Fig.1 for example, should be specified for accurate prediction of device characteristics such as Id-Vg, Id-Vd and C-V. Monte Carlo simulations (Kunitomo et al. 1999) and response surface methods (Felt et al. 1996), which are well-known methodologies for predicting the distribution, have a problem in that they cannot specify the typical process conditions which lead to particular device characteristics.

We have developed a new methodology for predicting the distribution of device characteristics, which also enables us to specify the most typical process conditions for any device characteristics with only a few calculations. In our approach, to obtain the total distribution and process conditions, arrays which represent the distribution of the device characteristic caused by the fluctuation of every single process are prepared and then merged.

2. Methodology for Predicting the Distribution of Device Characteristics

Before applying our method, well-calibrated process and device simulators should be prepared. The method consists of the following four steps:

(step 1) Processes which have significant effects on the device characteristic, saturated drain current IdsN and IdsP in this case, are selected by calculating sensitivities of every process fluctuation to the characteristic. From this result, the distribution of every selected process is mapped onto the distribution of the device characteristic.

(step 2) For every process selected, a two dimensional array with IdsN and IdsP for row and column is prepared. Elements of the arrays are filled with probability of occurrence of the corresponding IdsN-IdsP value pairs calculated from the distribution of the device characteristic.

(step 3) Arrays for every significant process specified in step 2 are merged. Elements of the merged array are calculated using the following equation:

$$P_{p1,p2}(i,j) = \sum_{m,n}(P_{p1}(m,n) * P_{p2}(i-m, j-n))$$

where $P_p(i,j)$ is the probability of occurrence of the (i,j) element, with the origin specified at nominal values of IdsN and IdsP, caused by the fluctuation of process p. This operation represents that assuming process p1 and p2 are independent, every element of the array caused by process p2 is distributed following the distribution of another process p1. In the computational implementation of this operation, every array element has an attribute list, where the corresponding process name, value and probability of occurrence are described. These lists are then combined and passed to the resultant array during the operation, which enables us to predict the most typical process conditions for the specified IdsN-IdsP value pair.

(step 4) To specify an appropriate 3σ or any distribution area from the resultant array, elements with a higher probability of occurrence are selected from the array and added until the sum of the probability reaches the specified rate. When the 3σ area is specified, the values of the array elements are added until the sum reaches 99.7%.

3. Application Example

We have applied this method to predicting the distribution of the IdsN-IdsP characteristics of a 0.18μm generation MOSFET and then evaluated our method by comparing the resultant distribution with the measured data and data calculated using Monte Carlo simulation.

3.1. Specification of Device Characteristics Distribution

We have analyzed the sensitivity of a device characteristic of saturated drain current (IdsN and IdsP) to every process fluctuation, and three major processes whose fluctuations have significant effect on the characteristic are selected. The nominal values and standard deviation (3σ) of the processes and their effect on the characteristic are shown in Table 1. Though every process fluctuation is assumed to follow Gaussian distribution, distribution of the characteristic caused by Lg fluctuation does not because of the non-linearity of the drain current vs. gate length relation. We specified two separate Gaussian distributions of the characteristic, one for the case gate length is manufactured longer than the nominal, and the other for shorter. Gate length mismatch represents the difference between the gate lengths of paired NMOS and PMOS; the distribution of the characteristic caused by the mismatch depends on the gate lengths of the pair because of short channel effects. We specified the distribution of the characteristic caused by gate length mismatch as a function of Lg.

3.2 Calculation Results and Their Accuracy in Re-calculation

Calculation results are shown in Fig.2 with 1σ, 2σ and 3σ distributions indicated. Most typical process conditions that lead to FF, SS, FS and SF points on the 3σ line are extracted and shown in Table 2. With these process conditions, device characteristics are calculated again and compared with the original prediction (Fig.3 and Table 3). All differences are less than 2%, which indicates the degree of accuracy of our method for the extraction of process conditions which lead to particular device characteristics.

3.3 Comparison with Measured Data and Monte Carlo Simulation

The 3σ line derived using our method is shown with the calculated points using Monte Carlo simulation (1,000 points, Fig.4) and the measured points of manufactured chips (11,649 points, Fig.5). Compared with Monte Carlo simulation, 99.3% of calculated points are within our 3σ line and its distribution indicates good agreement with our method. As for the measured data, 99.3% of the measured points are within our 3σ line and its distribution tends to shift slightly in the direction of less Ids, compared with our method. These comparison results suggest that our method provides sufficient accuracy in the development phase.

4. Conclusion

We have developed an efficient method to predict the distribution of device characteristics. Using this method, not only the distribution but also the typical process conditions for any particular device characteristics can be extracted from the result. Comparison with the result of Monte Carlo simulation and with the measured data has established that our method is accurate and practical.

References

Kunitomo,H., Sato,H., Tsuneno,K., Ikematsu,R., Masuda,H. (1999): "TCAD Prototyping with New Accurate Worst-Case Definition for a 0.2 Micron CMOS ASIC Process," 4th IWSM, pp.38-41, 1999 4th IWSM, pp.38-41

Felt,E., Zanella,S., Guardiani,C., Vincentelli,A.S. (1996): "Hierarchical Statistical Characterization of Mixed-Signal Circuits Using Behavioral Modeling," Proc. IC-CAD, pp.374-380, 1996 Proc. IC-CAD, pp.374-380

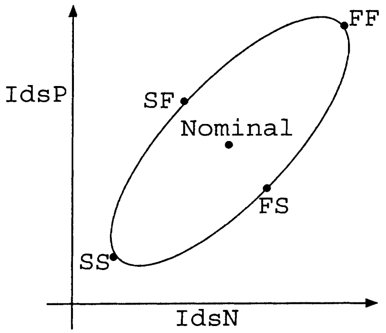

Fig.1 Measured distribution outline of IdsN-IdsP pairs. Nominal point is for center values of IdsN and IdsP. FF stands for NMOS Fast and PMOS Fast, SS for NMOS Slow and PMOS Slow, and so on.

Table 1 Fluctuations of three major processes, and their effect on IdsN and IdsP.

Process fluctuations	nominal	standard deviation (3σ)
Lg	0.15μm	0.015μm
Lg Mismatch	0μm	0.0056μm
Tox	3.47nm 3.67nm	0.069nm (NMOS) 0.073nm (PMOS)
Nominal values of IdsN and IdsP(mA/μm)		
NMOS	5.60	
PMOS	1.97	
Calculated deviations(3σ) caused by single process fluctuations(mA/μm)		
Lg	IdsN 1.22(shorter),0.836(longer) IdsP 0.389(shorter),0.27(longer)	
Lg Mismatch	$IdsN(Lg)=158Lg^2-55Lg+5.0$ $IdsP(Lg)=-17Lg^2+3.2Lg$	
Tox	IdsN 0.158 IdsP 0.101	

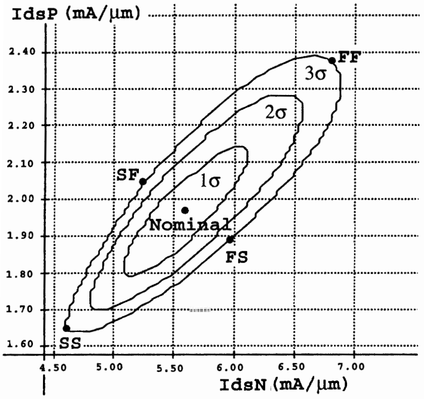

Fig.2 Calculated distribution of IdsN-IdsP pairs and FF,SS,FS and SF points on 3σ outline.

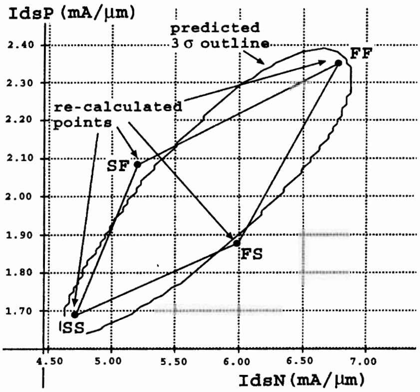

Fig.3 Comparison of re-calculated device characteristics with the distribution of the original prediction.

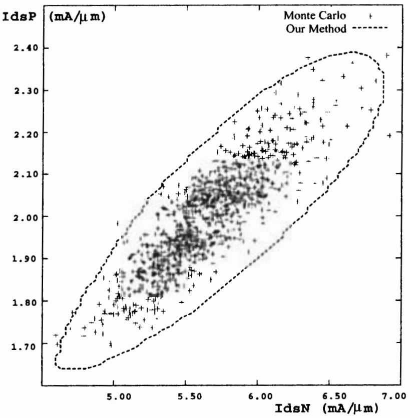

Fig.4 Distribution calculated by Monte Carlo Simulation (cross) and 3σ outline by our method (line).

Table 2 Most typical process conditions predicted with our method, that lead to FF, SS, FS and SF points in Fig.2.

FF: IdsN:6.8-6.835, IdsP:2.37-2.38(mA/μm)
Lg(μm) N:0.1356 , P:0.1356
Lg Mis(μm) N:0, P:0
Tox(nm) N:3.451 , P:3.65
SS: IdsN:4.665-4.7, IdsP:1.64-1.65(mA/μm)
Lg(μm) N:0.1654 , P:0.1654
Lg Mis(μm) N:-0.0003774 , P:0.0003774
Tox(nm) N:3.493 , P:3.694
FS: IdsN:5.89-5.925, IdsP:1.87-1.88(mA/μm)
Lg(μm) N:0.1490 , P:0.1490
Lg Mis(μm) N:-0.005358 , P:0.005358
Tox(nm) N:3.483 , P:3.684
SF: IdsN:5.26-5.295, IdsP:2.05-2.06(mA/μm)
Lg(μm) N:0.1512 , P:0.1512
Lg Mis(μm) N:0.005585 , P:-0.005585
Tox(nm) N:3.460, P:3.660

Table 3 Difference of re-calculated saturated current (IdsN and IdsP) compared with original prediction at FF,SS,FS and SF points.

	FF	SS	FS	SF
IdsN	-0.6%	0.8%	1.4%	-1.1%
IdsP	0.4%	1.0%	0.4%	1.5%

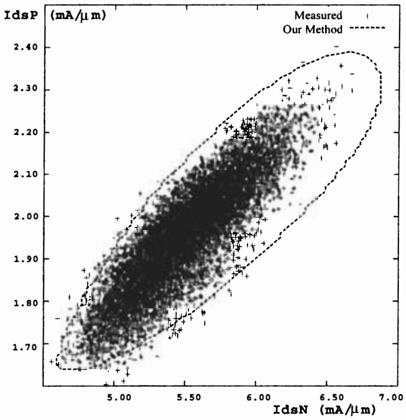

Fig.5 Measured distribution (cross) and 3σ outline predicted by our method (line).