Statistical Analysis of VLSI Using TCAD

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Abstract

Statistical process fluctuations influence upon device and circuit performance of VLSI with device miniaturization. Thus, robust process, device and circuit designs are needed. This article describes the statistical analysis of MOSFET and interconnect using Technology CAD (TCAD).

1 Introduction

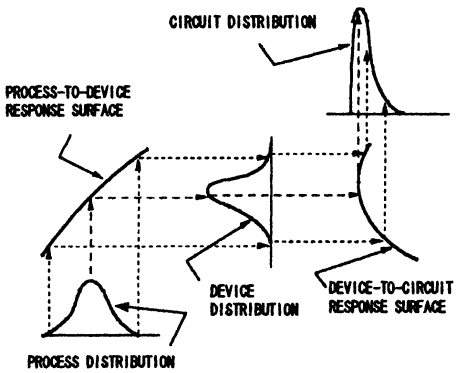

Fig. 1 Process fluctuation and circuit performance [2].

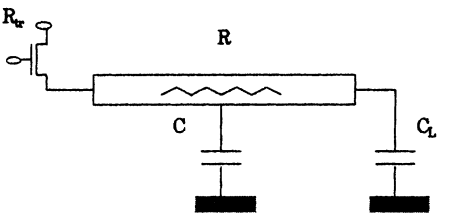

Fig. 2 Variability of device and interconnect.

The dependence of the parametric yield of VLSI on statistical process fluctuations such as a critical dimension (CD) and an ion implantation, has been increased. The statistical simulation is needed for robust designs of process, device and circuit [1].

Fig. 1 shows a schematic explanation of the relation between the process fluctuation and circuit performance [2]. The process fluctuation is related to device performance through a process-to-device *response surface*. The device performance is related to circuit performance through a device-to-circuit response surface. Process/device simulators can be used for representing the process-to-device response surface. Also, a circuit simulator is used for the device-to-circuit response surface.

This article presents TCAD based statistical analysis for the variability of device and interconnect, as shown in Fig. 2. The circuit delay t_{delay} is approximated as 2.3 $R_{tr}C$ + RC where R_{tr} is the MOSFET resistance [3]. In the case of short interconnect length

L, $R_{tr}C$ dominates t_{delay}. On the other hand, the interconnect RC delay dominates t_{delay} for long L. In Section 2, the worst case circuit model for MOSFET and problems for the statistical simulation are described. The interconnect variability is treated in Section 3.

2 Device Variability: MOSFET

2.1 Worst case circuit model

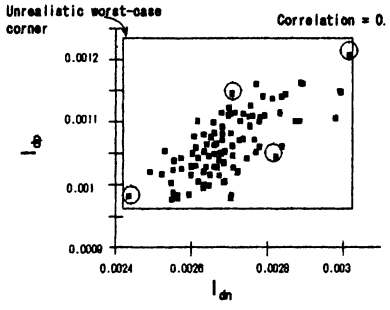

Fig. 3 Unrealistic worst-case corners [4].

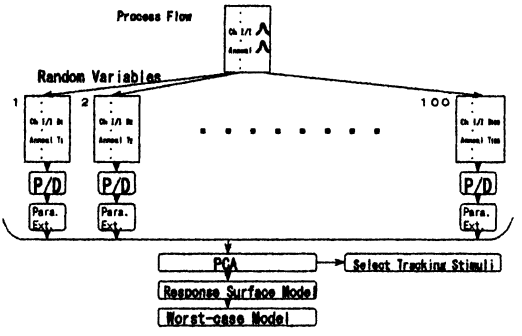

Fig. 4 Schematic explanation for statistical analysis and generation of worst-case models [5].

Fig. 3 shows a scatter plot of the n-ch and p-ch saturation drain current, I_{dn} and I_{dp} [4]. A circuit designer has used min-max worst-case corner models. In this example, however, there was a strong correlation between I_{dn} and I_{dp}, whose correlation coefficient was 0.71. Thus, the upper-left and lower-right corners were *unrealistic* worst-case corners.

Fig. 4 shows a schematic explanation for the statistical analysis and generation of worst-case BSIM3v3 models [5]. Before Monte Carlo (MC) runs, process conditions for a simulation were assigned separately to each process step using random numbers with assuming process fluctuations of the normal distribution. The number of MC runs is related to the accuracy [6].

MC runs resulted in 97 sets of BSIM3v3 parameters. At each run, a set of 144 (= 72 × 2) model parameters for n-ch and p-ch MOSFET's was extracted. Hence, 97 points which corresponded to the extracted parameter sets, were placed in a 144-dimensional space; a BSIM3v3 space. Independent *factors* were selected using the principal component analysis (PCA) [7]. Then, tracking stimuli were selected from the process variables, which had strong correlation to the factors. Finally, the response surface model (RSM), hence the worst-case models were generated as combinations of the tracking stimuli using the values of σ for the process variables. It is noted that the conventional method gives the worst-case models in the sense of the

corners of the *process* fluctuations, so that they do *not always* correspond to those for the circuit performance, as shown in Fig. 1.

Table 1 shows 11 factors, which were needed to cover the 80 % of the BSIM3v3 space. An increase in the number of factors m enlarges the coverage of the BSIM3v3 space. However, this results in an increase in the worst-case corners, hence, the number of required circuit simulations. For example, 128 ($= 2^{11-4}$) circuit simulations are required even using the design-of-experiments (DOE) of resolution V. For a large circuit, a reduction of m is important to decrease the circuit simulation time.

The total coverage of BSIM3v3 space using factors 1, 2 and 3 was only 43 %. In order to supplement the small coverage, the factors were selected not by its coverage, but by its sensitivity to the performance of a small but critical circuit. The *sensitivity* analysis was carried out for reducing m. A ring-oscillator was used as an example.

Fig. 5 shows the sensitivities of the factors to the delay time *tpd* with ± 3σ process fluctuations. The characters of the lateral axis indicate the sign of each factor. For example, *f01+* means that factor 1 was changed +3σ from the nominal value. The short-channel effect was pronounced in the case of *f01+*. Factors 2, 1, and 8 had higher sensitivities to *tpd*, where the tracking stimulus for factor 8 was the gate oxidation temperature. On the other hand, factor 3 (LDD spacer) had a small contribution to *tpd*. This is because LDD spacer is related to

Table 1 Tracking stimuli and coverage of BSIM3v3 space for the factors [5].

Name	Tracking Stimulus	Coverrage of BSIM3 Space [%]
Factor 1	Gate CD	19
Factor 2	P-ch As I/I Dose	12
Factor 3	LDD Spacer Thickness	12
Factor 4	N-ch B I/I Dose	8
Factor 5	Gate Oxidation Time	7
Factor 6	N-ch LDD I/I Dose	6
Factor 7	P-ch B I/I Dose	4
Factor 8	Gate Oxidation Temp.	4
Factor 9	SiN Depo. Thickness	4
Factor 10	None	3
Factor 11	Dummy Oxidation Time	2

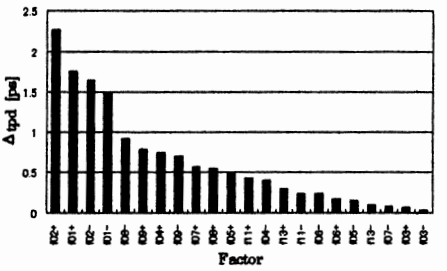

Fig. 5 Sensitivities of factors to delay time *tpd* [5]. $|V_{DS}| = 3.3$ V, W / L = 5 / 0.3 for n-ch, and W / L = 10 / 0.3 for p-ch.

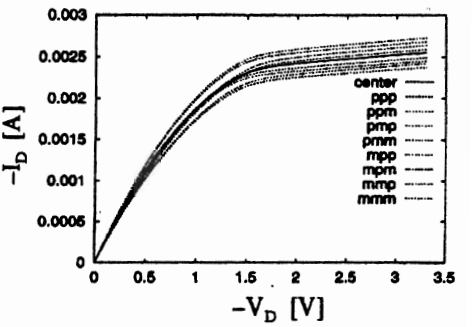

Fig. 6 I_D-V_D characteristics of p-ch MOSFET's using nine BSIM3v3 worst-case models [5]. $V_{GS} = -3.3$ V, $V_{BS} = 0$ V and $W/L = 10/0.3$.

both the source/drain sheet resistance and the overlap capacitance. There was a tradeoff between the two, so that factor 3 had small influence on *tpd*. Factors 1, 2, and 8 were selected for reducing *m*. In general, the factor with high coverage of the BSIM3v3 space does not always correspond to the high sensitivity to the circuit performance.

Fig. 6 shows the p-ch I_D-V_D characteristics of the nominal and 2^3 worst-case models using factors 1, 2, and 8, based on $\pm 3\sigma$ process fluctuations. Factor 1 (CD) had large influence on both I_{dn} and I_{dp}. Factor 2 (p-ch As I/I dose) had largest influence on I_{dp} due to the buried-channel structure of p-ch MOSFET's ($L = 0.3$ μm).

2.2 Tasks for statistical simulation

The following list describes problems for realizing the statistical simulation.
(1) Definition of the worst-case model in the sense of circuit performance [8].
(2) Estimation of the standard deviation σ of the process fluctuation.
(3) TCAD predictability.
(4) Numerical noise such as the meshing noise [9] .

The problem (4) is treated in this article. The meshing noise is very crucial problem for the sensitivity and statistical analysis.

Fig. 7 shows the threshold voltage V_{th} as a function of the channel length L [9]. There were discontinuities in V_{th}. This is so-called meshing noise. The meshing noise is due to the change in the potential barrier between the source and channel, which is induced by the abrupt change in mesh points along the lateral direction. The default mesh was automatically generated. Hence, the abrupt change in the number of mesh points at some L caused these V_{th} discontinuities. There were only five mesh points in the channel (solid line). When fixing the number of mesh points in the channel as 20 (broken line), a real potential barrier was obtained. The difference in a maximum potential barrier between default and fixed meshes was 18 mV, which corresponded to the discontinuity in V_{th}. This is a typical example of the meshing noise.

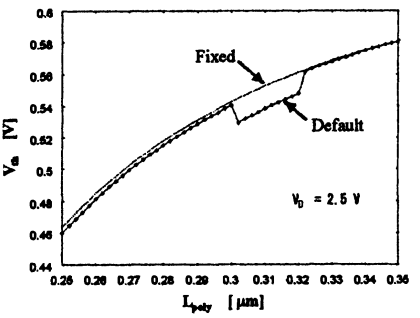

Fig. 7 shows the threshold voltage V_{th} as a function of the channel length L [9].

The mesh generation should be based on physics considering the relation between the mesh size and the physical quantities in order to reduce the meshing noise. Here, the mesh dependency of the inversion carrier density N_{inv} [10] and the surface roughness mobility μ_{surf} [11] are discussed, which are very important for MOSFET simulation.

The mesh dependency of N_{inv} was investigated by Tanimoto and Shigyo [10]. Fig. 8 shows the N_{inv}-V_G characteristics for different grid size, where one-dimension simulation was used with constant grid size. Here, Delaunay and Voronoi meshes were used for the comparison. Device simulators have usually used Delaunay mesh, where the grid locates at the surface of the silicon substrate. On the other hand, the boundary of the control volume (CV) is locates at the surface for Voronoi mesh. As show in the Fig. 8, Delaunay mesh overestimated N_{inv}. Voronoi mesh underestimated it. These can be explained using Fig. 9. Delaunay mesh overestimated the number of carriers in the control volume at the surface, hence N_{inv}.

Fig. 10 shows minimum grid size to ensure the accuracy of N_{inv} for Delaunay mesh. Less than 1 nm grid is required to ensure 10% accuracy of N_{inv} in the subthreshold region for the substrate concentration N_A of $2 \times 10^{17}\,cm^{-3}$.

Fig. 11 shows the channel conductance as a function of grid size. Watt's model [12] considered the universality of μ_{surf} only by one girid at the surface. Thus, this model overestimated μ_{surf} with a decrease in the grid size, since the mobility at the next grid to the surface was considered to be bulk one. Shin et al. [13] proposed the method, which solved this problem. Their method provided a linkage between the *local* and *effective* mobility. Their method is mathematically correct, but it requires a fine mesh.

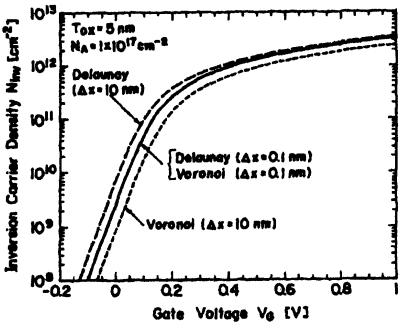

Fig. 8 Inversion carrier density N_{inv} as a function of gate voltage V_G [10].

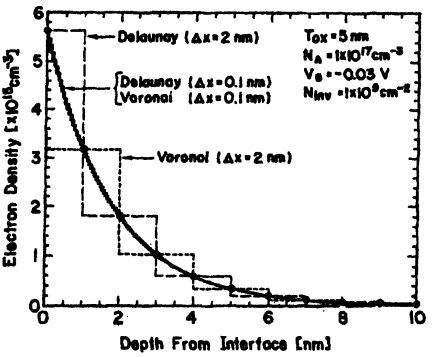

Fig. 9 Electron density as a function of depth [10]. Delaunay grid overestimated N_{inv}.

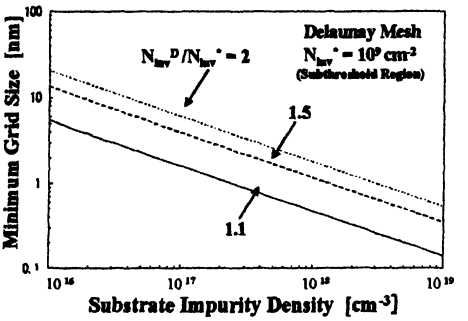

Fig. 10 Minimum grid size to ensure accuracy of N_{inv} for Delaunay mesh.

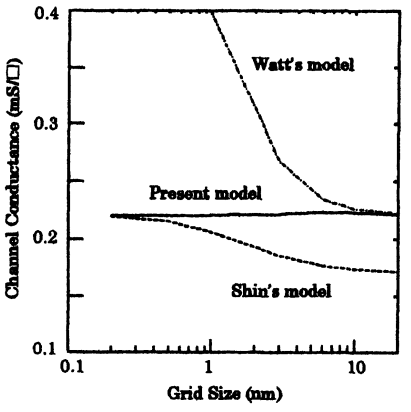

Fig. 11 Channel conductance as a function of grid size.

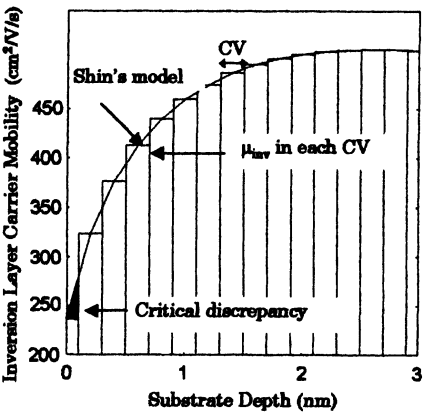

Fig. 12 Inversion carrier mobility as a function of depth [11].

Fig. 12 shows the cause of the grid size dependency. The major problem is the estimation of μ_{surf} at the surface. Enda and Shigyo [11] modified Shin's model with physical consideration. The vertical electric field E_V in the surface control volume was estimated using the values of E_V at the surface and next grids. Using this formulation, the grid size dependence on μ_{surf} could be reduced, as shown in Fig. 11.

3 Interconnect Variability

The importance of the interconnect RC delay is becoming larger with the advance in VLSI. Fig. 13 shows the interconnect structure used for the analysis. Periodic lines [14] were used. In the analysis, the vertical scaling for the interconnect height H and thickness T was not considered for the simplicity. A two-dimensional simulator [14] with 100 x 70 mesh points was used to calculate C.

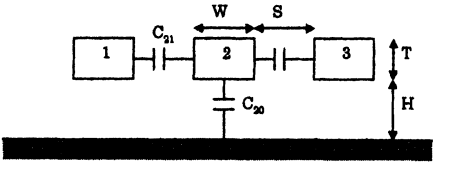

Fig. 13 Interconnect structure. T/H = 0.6.

Fig. 14 shows the relative variation of $\Delta C/C$ for +10% $\Delta W/W$. The space S was equal to $W - \Delta W$. The parallel plate capacitance C_P was calculated as $C_P/(\kappa_{ox}\varepsilon_0 L) \equiv W/H + 2\,T/S$, where κ_{ox} is dielectric constant of oxide, and ε_0 permittivity of free space. It is found that the simulated relative variation $\Delta C/C$ was *smallest* when $W/H \approx 2$, because of the fringing capacitance C_F, which is a parasitic component originated from the fringing

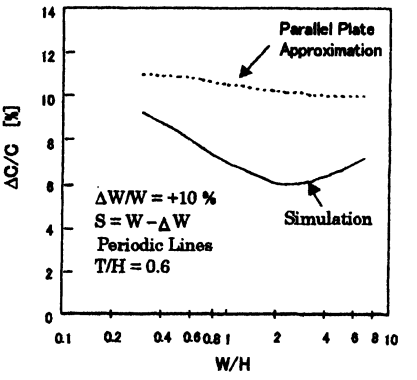

Fig. 14 Capacitance variation $\Delta C/C$ for +10 % CD variation, $\Delta W/W$ [15].

electric field. C_F reduces ΔC.

Fig. 15 shows the relative variation of $|\Delta(RC)/(RC)|$ for +10% $\Delta W/W$. *Maximum* variation occurred when $W/H \approx 2$, which was opposite to the minimum case for $\Delta C/C$. There is a *tradeoff* between $\Delta C/C$ and $\Delta(RC)/(RC)$. The RC delay variation is decomposed as follows.

$$\frac{\Delta(RC)}{RC} = \frac{(R+\Delta R)(C+\Delta C)-RC}{RC} = \frac{\Delta R}{R}+\frac{\Delta C}{C}+\frac{\Delta R \Delta C}{RC}. \quad (1)$$

In Fig. 15, $|\Delta(RC)/(RC)|$ was less than 1 % for the parallel plate approximation. This is because the resistance variation $\Delta R/R$ was cancelled by $\Delta C/C$, i.e., there is a *negative correlation* between the two. In the actual case, C_F reduced $\Delta C/C$, so that $\Delta R/R$ was *not* canceled by $\Delta C/C$. Fig. 16 shows each component of (1). The value of $\Delta R/R$ was constant so that the decrease in $\Delta C/C$ due to C_F resulted in the increase in $|\Delta(RC)/(RC)|$.

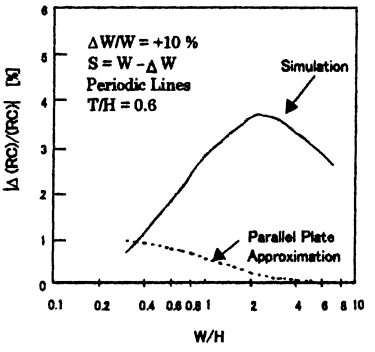

Fig. 15 RC delay variation $\Delta(RC)/(RC)$ for +10 % CD variation, $\Delta W/W$ [15].

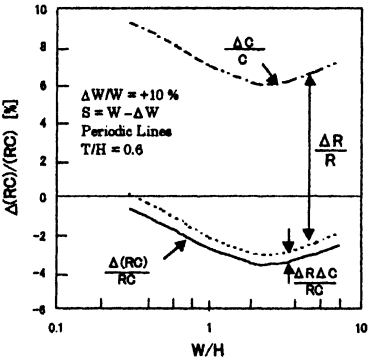

Fig. 16 Each component of (1).

An interconnect design guideline to reduce C and/or RC delay variations is as follows. In the case of short interconnects, $R_{tr}C$ is crucial for the circuit delay, so that the fringing ratio F ($\equiv C_F/C_P$ where $C_F \equiv C - C_P$) should be *large* to reduce the C variation. On the contrary, F should be *small* for long interconnects to reduce the RC variation.

4 Conclusion

The robust designs of process, device and circuit are crucial for realize VLSI, since process fluctuations influence upon device and circuit performance. The statistical simulation using TCAD is one of methods to solve this problem. An example of the generation of MOSFET worst-case circuit models using TCAD was demonstrated. An analysis of the variability of the interconnect reveled that there is a *tradeoff* between $\Delta C/C$ and $\Delta(RC)/(RC)$ because of C_F. TCAD based statistical analysis become increasingly importance. The meshing noise should be solved with physical considerations.

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