Two-Dimensional Diffusion Characterization of Boron in Silicon using Reverse Modeling

Eitan N. Shauly
Faculty of Materials Engineering, TECHNION-Israel Institute of Technology, Haifa 36000, Israel and Tower Semiconductor Ltd, Migdal Ha'Emek 10556, P.O.B. 619, Israel,
(email: cezsmh@TowerSemi.com)

Richard Ghez and Yigal Komem
Faculty of Materials Engineering, TECHNION-Israel Institute of Technology, Haifa 36000, Israel

Abstract

This work deals with the simulation of two-dimensional impurity diffusion in CMOS silicon devices. The Reverse Modeling method was used to determine the diffusion coefficient (D_I), surface recombination rate of defects (K_I) and the characteristics of the injecting source. Analysis showed similarity between D_I in 2-D system compared with the value obtained from non-patterned samples. The results for D_I and K_I are very well described by the Arrhenius expressions. D_I was found to be related to the substrate type e.g. EPI or CZ. The values of K_I related to the interface type, oxidizing or non-oxidizing (SiO_2 or Si_3N_4).

1 Introduction

Simulation of semiconductor device structures requires modeling the underlying physics of semiconductor fabrication processes. The need for accurate simulation becomes more critical with the growing complexity of design and the continuing reduction in device dimensions. For this reason much effort has been invested in determining the values of model parameters, which give good predictive capability. The primary goal of this work is to develop a Reverse Modeling concept, which can be used to determine model parameters that cannot be measured directly. This method was used to study 2-D impurity diffusion in CMOS silicon devices, and the interaction between point defects and diffusing species. The parameters determined were the diffusion coefficient (D_I) and surface recombination rate of interstitials (K_I) and the characteristics of the injecting source, θ, that represents the amount of Si atoms consumed during oxidation and injected as intertistals down into the bulk.

2 The Reverse Modeling concept

The Reverse Modeling concept enables studying process parameters and is based on statistical comparison between 2-D process and device simulations and various electrical and physical measurements of sub-micron devices. A process simulator was used to compute the physical characteristics of a CMOS device. Using this data, a device simulator was used to predict electrical characteristics, which were compared with measurements of real devices. The comparison was used as feedback to update the process simulator, until a reasonable agreement was reached. Unlike function fitting, this concept does not require a direct measurement of the studied parameters.

3 Parameters for point defect diffusion and recombination

The physical mechanism of atomic diffusion is similar in all semiconductor systems. However, the complexities of devices, introduce new boundary conditions for the diffusing elements. For example, in cases where part of an implanted layer was covered by nitride capping before

oxidation, three types of diffusion conditions need to be studied: under the cover, in the oxidized area and in the transient zone around the blocking edge.

It is generally accepted that injection of silicon atoms from the growing oxide lead to oxidation enhanced diffusion (OED). The injected interstitials will diffuse, like any other element, having temperature depended diffusivity (D_I). Some interstitials that reach an interface, will recombine at the "recombined surfaces" having a surface recombination rate K_I. Assuming no generation or presence of vacancies, one can specify a linear combination of flux and field at the boundary:

$$D_I \nabla C_I - K_I \left(C_I - C_I^*\right) = 5 \times 10^{22} \theta \left(\frac{dx}{dt}\right)^S \qquad (1)$$

where C_I and C_I^* are the local and the equilibrium concentrations of interstitials, respectively. The left hand-side of equation 1 is the "thermodynamic force" (∇C_I) or the "driving force for diffusion" ($D_I \nabla C_I$) into the silicon bulk [1]. The right hand-side, represents the surface injection flux, where θ is the percentage of consumed silicon lattice atoms that are injected back into the silicon bulk as interstitials, and dx/dt is the oxide growth velocity. The power S depends on the oxidation conditions with typical values of 0.3-0.6 [2].

The values of D_I, K_I and θ are hard to obtain, since they can found only through modeling of another phenomena, like OED [3, 4] or Oxidation Induced Stacking Faults (OISF) [5]. K_I, values can only be extracted using special test structure [12, 6]. A literature review for the values of D_I, K_I and θ showed considerable scatter in results up to several orders of magnitude.

4 Experimental details and calculation methods

The study was initiated by tuning the process and device simulators by 1-D process modeling adjustment, using results of 1-D SIMS, thickness, and sheet resistance measurements. 2D electrical modeling for the mobility and threshold voltage was adjusted based on long channel device measurements.

The bulk of the work included experiments performed under different process conditions namely heat treatment under N_2 or dry O_2 atmospheres, at different temperatures. Submicron CMOS devices were fabricated using 0.8μ technology, with gate lengths in the range of 1.6μ to 0.56μ, full details are given by Shauly [7]. 2-D process and device simulations were executed using SUPREM-IV [8] and MEDICI [9], respectively. A large matrix of simulations was run using the principles of statistical design of experiments, to find the values of D_I, K_I and θ. This matrix enabled fitting a quadratic model for each one of the electrical parameters to quantify it's sensitivity to the post implantation heat treatment conditions. A large number of electrical testing (ET) parameters were measured including transistor drive current, threshold voltage, transistor peak substrate current and more. For each of the matrix simulation runs, the response value (Δ) was calculated, to evaluate the difference between simulation and experimental results.

$$\Delta = \frac{\left(\mathrm{O}_{\text{simulation}} - \mathrm{O}_{\text{experimental}}\right) - \left(\mathrm{N}_{\text{simulation}} - \mathrm{N}_{\text{experimental}}\right)}{\mathrm{SCALE}} \qquad (2)$$

where "O" refers to the values obtained under oxidation conditions, and "N" to the values obtained at N_2 ambient conditions. To facilitate a joint solution for more than one ET parameter, the observed Δ was also scaled by dividing by a predetermined scaling factor for each ET parameter.

5 Results and discussion

The accuracy of the simulation system was verified using a series of transistors implanted with different *p*LDD doses and annealed under N_2 ambient. The measured and simulated values of electrical parameters of these transistors were equal within experimental error. This gave confidence that simulation system describes well the devices fabricated with N_2 anneal. Based on this, it was concluded that the results obtained to describe OED using the Reverse Modeling concept do reflect the effects of O_2 in the anneal ambient.

Using surface response method and setting Δ equal to 0, values for D_I, K_I and θ were found. Over the temperature range of 800°C - 950°C, the results for D_I and K_I are very well described by the Arrhenius expressions:

$$D_I = 1.06\times10^{-4}\exp\left(\frac{-1.32\text{eV}}{kT}\right) \quad \text{cm}^2/\text{sec} \tag{3}$$

$$K_I = 1.26\times10^{-11}\exp\left(\frac{+1.65\text{eV}}{kT}\right) \quad \text{cm}/\text{sec} \tag{4}$$

The typical value of θ in this temperature range was found to be 0.01. The parameter showed weak dependence on temperature. To validate these results, B profiles after oxidation, as measured using SIMS, were compared with 1-D simulated profiles and D_I was extracted. Analysis showed similarity between D_I in 2-D system compared with the value obtained from non-patterned samples (Fig 1). Since the intestinal diffusivity in the bulk does not depend on the nature of the interface surrounding the bulk, the values obtained for D_I were similar (see lines c& d). Comparison with results from the literature showed similarity to results obtained by some researchers (lines e & f), and pronounced differences compared with others (lines a & g). Careful examination of the data showed that D_I depends on the substrate material. We verified experimentally this assumption and showed that D_I in samples having epitaxial (EPI) top layer, is higher by a factor of 3 compared to Czochralski (CZ) samples. A model for bulk trapping which affects D_I was proposed. Interactions of interstitials with traps located in the bulk have reduced D_I. The fact that the bulk traps density is lower in EPI samples compared to CZ, explained the higher value of D_I found.

The activation energy for the surface recombination rate was found (Fig 2). The variations between the values of K_I were attributed to the dependence of K_I on interface type (Table 1). The difference was explained for the first time, by stress induced from the upper layers, into the silicon substrate. Experiments showed that K_I of samples having a strained Si_3N_4/Si layer was half an order of magnitude lower compared to samples with SiO_2/Si interface An explanation for the reduction in K_I with a rise in temperature was given by decomposition of SiO_2 molecules to $Si+O_2$. Some of the Si atoms have diffused and were trapped to the Si/SiO_2 interface, reducing K_I.

Finally, the equilibrium concentration of interstitials was calculated based on the $D_I C_I^*$ relation developed by [10]. This gave the ability to present a full set of parameters needed for simulation of 2-D diffusion of B in Si.

Table 1: K_I values at 900°C and activation energy values for various trapping interfaces

Reference	Interface Structure	K_I (cm/sec)	*Ea* (eV)
[2]	Si/SiO2	6.3×10^{-4}	-1.75
This work	Gate=150A, Poly=3250A	1.0×10^{-4}	-1.65
[4]	Pad~800A, Nitride=1200A	3.5×10^{-6}	-1.58
[6]	Pad=400A, Nitride=800A	1.5×10^{-7}	-0.89
[5]	Oxidation Induced Staking Faults	2.3×10^{-8}	+2.4

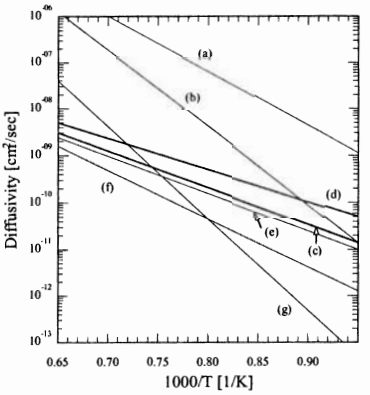

Fig. 1: Values for the self diffusivity (D_I) from the literature and this work. (a) [11]; (b) [12]; (c) 1-D, This work; (d) 2-D, This work; (e) [13, 8]; (f) [6]; (g) [5].

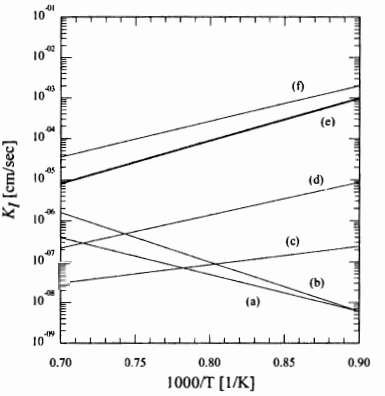

Fig 2: Interstitial recombination velocities, K_I, as determined experimentally at this work, and by other researchers. (a) [14]; (b) [5]; (c) [6]; (d) [13]; (e) 2-D, This work; (f) [2, 8].

6 Acknowledgements

The generous support of Tower Semiconductor Ltd. is gratefully acknowledged. The authors would also like to thank the Fund for the Promotion of Research at the Technion for partial support.

7 References

[1] Ghez, (1990): A primer of diffusion problems. John Wiley & Sons, New York.

[2] Dunham S. T. (1992): Interactions of silicon point defects with SiO2 films. J. Appl. Phys., 71:685-696.

[3] Griffin P. (1990): Physics and modeling of Two-Dimensional Diffusion in SUPREM-IV. PhD thesis, Stanford University.

[4] Kump, M. R., Dutton, R. W. (1988): The efficient simulation of coupled point defect and impurity diffusion. IEEE Trans. on Computer Aided Design, 7:191-204.

[5] Taniguchi, K., Antoniadis, D. A., Matsushita Y. (1983): Kinetica of self-Interstitials generated at the Si/SiO_2 interface. Appl. Phys. Lett., 42:961-963. See also: Taniguchi, K., Antoniadis, D. A., Matsushita Y. (1983): Kinetics of self-interstitials generated at the Si/SiO_2 interface. Appl. Phys. Lett., 42:961-963.

[6] Griffin, P. B., Plummer, J. D. (1986): Process physics determining 2D impurity profiles in VLSI devices. In Technical Digest, Intl. Elec. Dev. Mtng, Los Angeles, pp. 522-523.

[7] Shauly, E. N., (2001): A study of two-dimensional diffusion of dopants in CMOS devices. PhD thesis, Technion -Israel Institute of Technology, Haifa.Israel.

[8] SUPREM-IV, (1997): TSUPREM-IV Two-Dimensional Process Simulation Program ver. 6.5 User's Manual. Technology Modeling Associates Inc., Sunnyvale, Ca.

[9] MEDICI, (1997): MEDICI IV Two-Dimensional Device Simulation Program User's Manual Ver. 4.0. Technology Modeling Associates Inc., Sunnyvale, Ca.

[10] Morehead, F., (1988): Defects in electronic materials. Mat. Res. Soc. Symp. Proc., Pittsburgh, Pa., 104:9

[11] Bronner, G. B. & Plummer, J. D., "Gettering of gold in silicon: A tool for understanding the properties of silicon interstitials," J. Appl. Phys, 61(12), (1987), pp. 5286-5298.

[12] Griffin, P. B., Fahey, P. M., Plummer, J. D., Dutton, R. W. (1985): Measurement of silicon interstitial diffusivity. Appl. Phys. Lett., 47:319-321.

[13] Kump, M. R. (1988) Two-dimensional computer simulation of diffusion in silicon. Ph.D. Thesis, Stanford University, Palo Alto, Ca.

[14] Collard, D., Taniguchi, K. (1986): IMPACT - A point defect based two dimensional process simulator: Modeling the lateral oxidation enhanced diffusion of dopants in silicon. IEEE Tans. Elec. Dev., ED-33:1454-1462.